



Serial ATA International Organization

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Serial ATA Interoperability Program, Revision 1.4 Unified Test Document LeCroy MOI for RSG Tests Version 1.0 (Using PeRT³)



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MODIFICATION RECORD

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Chris Forker

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Chris Forker, David Li

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Chris Forker, David Li

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David Li

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David Li

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David Li

Aug 27, 2009 – RSG-05 changed from informative to Normative based on UTD1.4

David Li

Aug 27, 2009 – Version 1.0 (Approved by SATA Logo Workgroup)

David Li

INTRODUCTION

This document provides the method of implementation for testing the receiver of SATA devices as described in receiver testing portion of the Serial ATA Interoperability Program revision 1.3. A current copy of this specification can be found at www.serialata.org.

ACKNOWLEDGMENTS

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Detailed Tests

Purpose: Verify that the Product Under Test (PUT) meets the jitter tolerance requirements for Gen1, Gen2 and Gen3 products if they claim to support the associated speeds accordingly.

References:

- Serial ATA Specification, Revision 3.0
- Serial ATA Interoperability Program, Revision 1.4 Unified Test Document

Resource requirements:

See appendix A

Jitter Source Calibration:

- See appendix C for calibration and validation of the following:
 - o Transition time
 - o Rj
 - o Sj
 - o Tj
 - o Amplitude

Discussion:

All RSG tests involve putting the PUT into BIST-L Loopback and measure Framed Error Rate. The generator will output stressed data with the specified amounts of Tj consisting Rj and Sine Jitter and measure FER accordingly.

PeRT³ test script allows for automatic initialization through OOB, speed negotiation and put PUT into BIST-L Loopback mode for FER testing. See appendix D for initialization details. The PeRT³ can complete the operation from OOB to BIST-L and FER measurement without any additional equipment. Once in loopback mode, the following receiver jitter tolerance tests can be performed:

- RSG-01 – Gen1 (1.5Gbps) as defined in section 2.17.2 of Serial ATA Interoperability Program, Revision 1.4 Unified Test Document
- RSG-02 – Gen2 (3Gbps) as defined in section 2.17.3 of Serial ATA Interoperability Program, Revision 1.4 Unified Test Document
- RSG-03 – Gen3 (6Gbps) as defined in section 2.17.4 of Serial ATA Interoperability Program, Revision 1.4 Unified Test Document
- RSG-05 – Gen1 (1.5Gbps) as defined in section 2.17.3 of Serial ATA Interoperability Program, Revision 1.4 Unified Test Document

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- RSG-06 – Gen1 (1.5Gbps) as defined in section 2.17.1 of Serial ATA Interoperability Program, Revision 1.4 Unified Test Document

Gen1 products should meet the test requirements for RSG-01, RSG-05, RSG-06

Gen2 products should meet the test requirements for RSG-01, RSG-02, RSG-05, RSG-06

Gen3 products should meet the test requirements for RSG-01, RSG-02 and RSG-03, RSG-05, RSG-06

Test Setup:

If the PUT is a Drive, connect the test setup as shown in appendix B, figure 6

1. Connect the pair of Molex cables from the FE6 to the R6, connecting “D-IN[0]” to “D-OUT” and “D-OUT[0]” to “D-IN”.
2. Connect the matched length SMA pairs between the FE6 and the LeCroy TF-SATA-C Test fixture. Match “Data RX” with Rx and “Data TX” with Tx.
3. Power up both the R6 and the FE6 and wait for the R6 to boot up (about 15 seconds).
4. Start the LeCroy PeRT³ software on the PC.
5. Connect the Product Under Test (PUT) to the SATA breakout board as specified in figure 6.

If the PUT is a Host system, connect the test setup as shown in appendix B, figure 2

1. Connect the pair of Molex cables from the FE6 to the R6, connecting “D-IN[0]” to “D-OUT” and “D-OUT[0]” to “D-IN”.
2. Connect the matched length SMA pairs between the FE6 transmitter differential output to and the SATA Host OOB Board input. Match “Data Tx” with “Switch FE” and “Switch DUT” with Tx of TF-SATA-C Test fixture.
3. Connect the matched length SMA pairs between the SATA breakout board Rx with the FE6 Detector inputs. Match “SATA breakout Rx” to “Data Rx”.
4. Power up both the R6 and the FE6 and wait for the R6 to boot up (about 15 seconds).
5. Start the LeCroy PeRT³ software on the PC.
6. Connect the Product Under Test (PUT) to the SATA breakout board as specific in figure 7

Test Procedure

1. The software will connect to the hardware and self calibrate automatically, which may take up to 2 minutes.
2. In Main tab, select SATA as the Protocol, then select the testing Bit rate.
3. To validate that FER mode is working correctly, set amplitude to 400mV, turn all jitter sources off and select the COMP pattern in the Channel 1 tab:



Figure 1

4. In the Main Tab, click connect and verify FER mode is active
5. Click run and verify that Frames are counting, click Inject Error and verify Frame Error increase
6. To verify that PUT is in BIST-L loopback mode, disconnect PUT Tx from PeRT3 error detector and connect differential pair to digital oscilloscope. Using the SDA function of oscilloscope, measure Sj and record value. Turn on Sj in PeRT3 to 62MHz and 100ps and measure Sj value using oscilloscope. Verify that first Sj reading is equal to second Sj reading. This will ensure that signal is in retimed loopback mode.
7. Reconnect PUT Tx to PeRT3 error detector
8. In the Test Scripts section, select from one of the following preset Test Scripts accordingly. (Note: the difference in Drive and Host testing is the initialization sequence to put device into Loopback mode)
 - a. SATA RSG-01 Drive
 - b. SATA RSG-01 Host
 - c. SATA RSG-02 Drive
 - d. SATA RSG-02 Host
 - e. SATA RSG-03 Drive (Informative)
 - f. SATA RSG-03 Host (informative)
 - g. SATA RSG-05 Drive
 - h. SATA RSG-05 Host
 - i. SATA RSG-06 Drive (informative)
 - j. SATA RSG-06 Host (informative)
9. For each test, calibrate the generator source and jitter sources as specified in Appendix C of this document
10. Each test script applied the Patterns, Amplitude, and Jitter values as defined in the Serial ATA Interoperability Program, Revision 1.4 Unified Test Document

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Each Test script is described in detail below with respect to the spec requirements:

RSG-01:

- Protocol is selected as SATA
- Bit Rate is selected as 1.5Gbps
- SSC is off
- Initialization is selected as Loopback
- Pattern to SATA_Framed_COMP
- Set amplitude to 500mV
- Rj and Sj described in table 1
- Connect CIC test board to the differential Tx outputs of the PeRT³

Test Case	Test model	Test Pattern	Rj (jitter amplitude)	Sj (amplitude and frequency) and Duration
RSG-01 Drive RSG-01 Host	Gen1	Framed COMP pattern with new LBP section	8.57 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)	Sj = 180ps (270mUI) 10Mhz – 10Minutes 33Mhz – 10Minutes 62Mhz – 10Minutes 5Mhz – 10Minutes

Table 1

RSG-02:

- Protocol is selected as SATA
- Bit Rate is selected as 3.0 Gbps
- SSC is off
- Initialization is selected as Loopback
- Pattern to SATA_Framed_COMP
- Set amplitude to 500mV
- Rj and Sj described in Table 2
- Connect CIC test board to the differential Tx outputs of the PeRT³

Test Case	Test model	Test Pattern	Rj (jitter amplitude)	Sj (amplitude and frequency) and Duration
RSG-02 Drive RSG-02 Host	Gen2	Framed COMP pattern with new LBP section	4.285 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)	Sj = 90ps (270mUI) 10Mhz – 5Minutes 33Mhz – 5Minutes 62Mhz – 5Minutes 5Mhz – 5Minutes

Table 2

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RSG-03:

- Protocol is selected as SATA
- Bit Rate is selected as 6.0 Gbps
- SSC is off
- Initialization is selected as Loopback
- Pattern to SATA_Framed_COMP
- Set amplitude to 500mV
- Rj and Sj described in Table 3
- Connect CIC test board to the differential Tx outputs of the PeRT³

Test Case	Test model	Test Pattern	Rj (jitter amplitude)	Sj (amplitude and frequency) and Duration
RSG-03 Drive RSG-03 Host	Gen3	Framed COMP pattern with new LBP section	2.14 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)	Sj = 32ps (192mUI) 10Mhz – 2.5Minutes 33Mhz – 2.5Minutes 62Mhz – 2.5Minutes 5Mhz – 2.5Minutes

Table 3

RSG-05:

- Protocol is selected as SATA
- Bit Rate is selected as 1.5 + 350ppm Gbps
- SSC is off
- Initialization is selected as Loopback
- Pattern to SATA_Framed_COMP
- Set amplitude to 500mV
- Rj and Sj described in Table 4
- Connect CIC test board to the differential Tx outputs of the PeRT³

Test Case	Test model	Test Pattern	Rj (jitter amplitude)	Sj (amplitude and frequency) and Duration
RSG-05 Drive RSG-05 Host	Gen1 (1.5Gbps + 350ppm)	Framed COMP pattern with new LBP section	8.57 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)	Sj = 180ps (270mUI) 62 Mhz – 18 iterations of Frame COMP wfp

Table 4

RSG-06:

- o Protocol is selected as SATA
- o Bit Rate is selected as 1.5 – 350ppm Gbps
- o SSC is ON
- o Initialization is selected as Loopback
- o Pattern to SATA_Framed_COMP
- o Set amplitude to 500mV
- o Rj and Sj described in Table 5
- o Connect CIC test board to the differential Tx outputs of the PeRT³

Test Case	Test model	Test Pattern	Rj (jitter amplitude)	Sj (amplitude and frequency) and Duration
RSG-06 Drive RSG-06 Host	Gen1 1.5Gbps – 350ppm with ideal 5000ppm triangular downspread SSC at 33Khz modulation freq. Data Rate is between 1.5Gbps-5350ppm and 1.5Gbps – 350ppm	Framed COMP pattern with new LBP section	8.57 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)	Sj = 180ps (270mUI) 62 Mhz – 18 iterations of Frame COMP wfp

Table 5

11. The preset test scripts will automatically apply Rj and Sj at specified jitter amplitude and frequency for each test case. The test will run for specified amount of time and verified to exhibit no more than zero frame errors for all four Sj Frequencies. In the case where at least 1000 errors are observed during execution, the test will stop before the specified time.

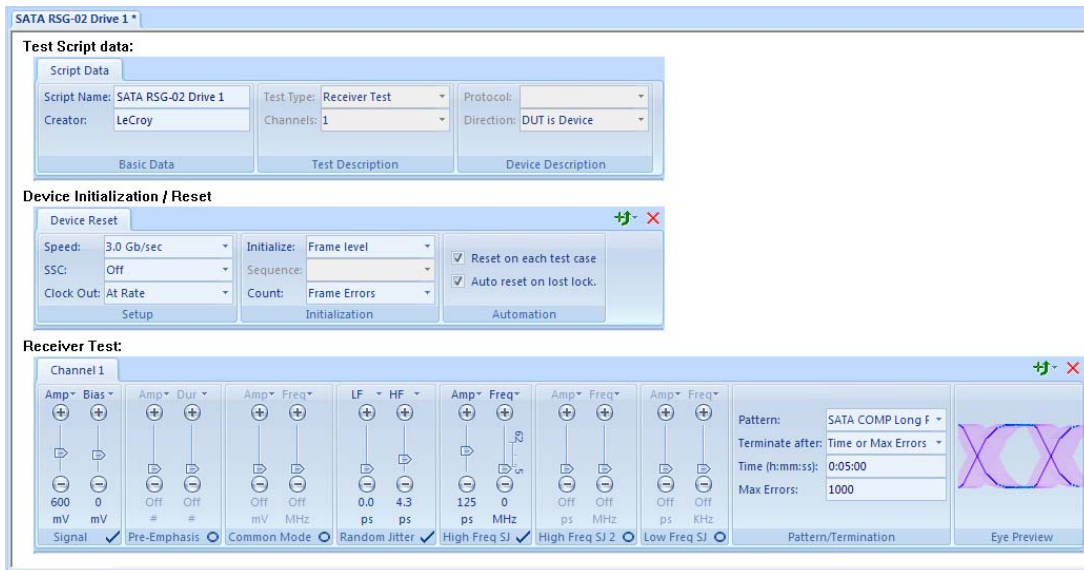


Figure 2 (Example of SATA RSG-02 Drive testing script)

Observe Results

Open the results file from the test and select scatter chart view:

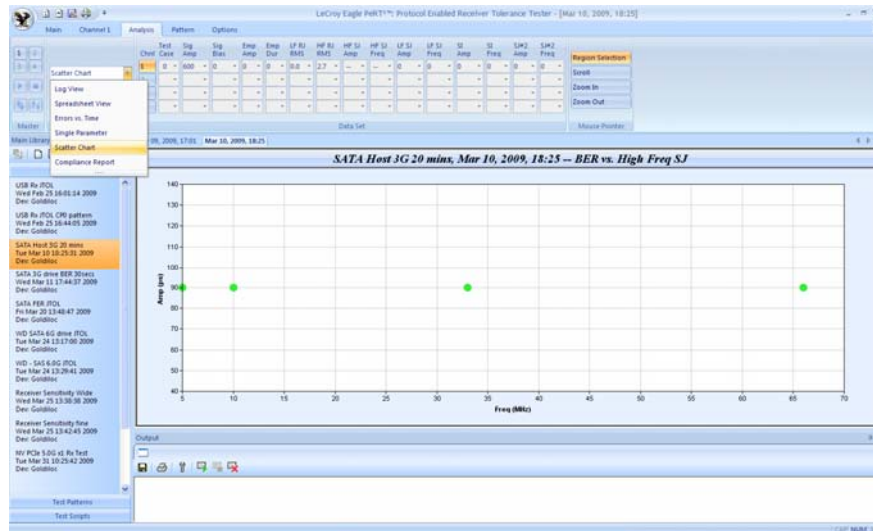


Figure 3

The result will show 4 data points at 5, 10, 33, and 62 Mhz of Sj with Sj jitter amplitude according to different test cases. Green shows pass with no errors; red shows fail with > 1 error in the test duration.

The spreadsheet view will provide the details testing log.

Possible Issues:

Some SATA host devices have different responses for electrical idle signals during Loopback operation, if PeRT³ fails to put device into BIST-L loopback mode for this reason, a LeCroy SATA Host Switch Board can be used to avoid switching delay which might affect Loopback operation. Figure to connect with the LeCroy SATA Host Switch Board can be found in Figure 7 under Test Setups.

Appendix A – Resource Requirements

The resource requirements include two instruments with accessories.

- 1) LeCroy Digital Oscilloscope (LeCroy SDA 816Zi for jitter source calibration)
- 2) PeRT³ 1 channel configuration (for all RSG testing)
 - PeRT³ system with the following options:
 - 1 PER-FE06-001-X (PeRT³ Eagle R6-8 1-Ch Front End)
 - 1 PER-R006-008-X (PeRT³ Eagle R6-8 Platform)
 - 1 SAT-R006-004-A (Eagle SATA Receiver Test Suite)
 - 1 PER-R006-008-A (Eagle Jitter Tolerance Test Suite)



Figure 4

- One PC with Windows XP or Vista and LeCroy PeRT³ software installed
- Two pairs of matched length SMA male to male cables
- LeCroy TF-SATA-C Test fixture

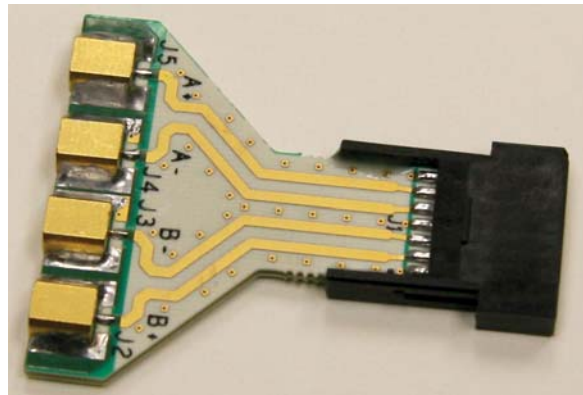


Figure 5

- 1 LeCroy SATA Host OOB Board
- 2 x Pico Second Pulse Labs 5915-110-100PS Rise Time Filters
- 1 LeCroy SATA CIC test board

Appendix B – Test Setups

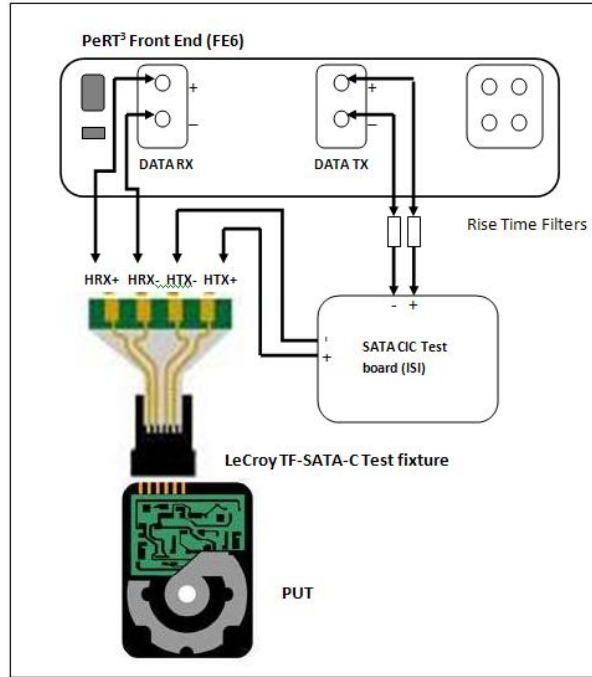


Figure 6 (Drive testing)

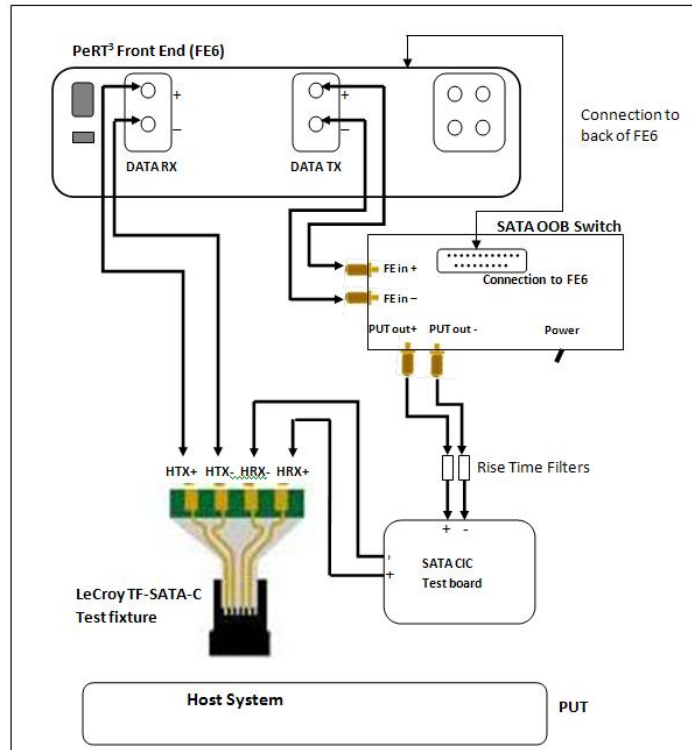


Figure 7 (Host testing)

Appendix C – Jitter Source Calibration

Propose: Calibrate and validate the PeRT³ generator output according the Gen1, Gen2 and Gen3 specification accordingly.

References:

- Serial ATA Interoperability Program, Revision 1.4 Unified Test Document

Resource requirements:

Please see Appendix A

Discussion: The test equipment must be calibrated each time before conducting RSG-01, RSG-02, and RSG-03 tests. The calibration process can be done using a real time digital oscilloscope. In this example, the LeCroy 816Zi DSO is used. The detailed test specification is described in table below:

Steps	Calibration Pattern	Method	RSG-01		RSG-02		RSG-03
			Gen1i	Gen1m	Gen2i	Gen2m	Gen3
Rise / Fall time	LFTP	Section 7.4.4 in SATA 3.0 Specification	100 ps (20/80%)		100 ps (20/80%)		62 ps to 75 ps (20/80%)
Rj	MFTP	Section 7.4.12 of SATA 3.0 Specification, Rj method also applied to Gen1i/m and Gen2i/m	8.57 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)		4.285 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)		2.14 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)
Sj	MFTP	Using Rj method defined in section 7.4.12 of SATA 3.0 Specification for all data rates	Sj = 180 ps (270mUI)		Sj = 90ps (270mUI)		Sj = 32ps (192mUI)
Tj	Framed COMP pattern with new LBP section	See UTD section 2.17.1.1	Tj(min) = 501 mUI Tj(max) = 519 mUI Using a channel that introduces 40 ps ± 6ps (i.e. min 36ps and max 46ps) of ISI in the given setup		Tj(min) = 552 mUI Tj(max) = 558 mUI Using a channel that introduces 40 ps ± 6ps (i.e. min 36ps and max 46ps) of ISI in the given setup		Tj(min) = 498 mUI Tj(max) = 570 mUI Using a CIC that introduces a min of 21ps and max 33ps of ISI in the given setup and that follows the

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							definition of section 7.2.7 of SATA 3.0 specification
Amplitude	Framed COMP pattern with new LBP section	For this test the amplitude distribution will be either measured or projected to a 1E-12 BER rates contour at the 50% location of the bit interval using previously calibrated edge rate and jitter. It is required to ensure that the maximum allowed voltage is not exceeded. Sections 7.4.3 and 7.4.12 of SATA 3.0 specification	325 mV	240 mV	275 mV	240mV	240 mV
			Maximum not to exceed peak to peak voltage of 600 mV		Maximum not to exceed peak to peak voltage of 750 mV		Maximum not to exceed peak to peak voltage of 1V

Table 6

Calibration setup:

- Connect the PeRT³ generator differential output to channel 1 and channel 2 on the LeCroy SDA 816Zi.
- In the PeRT³ software main tab, select Generator only option under protocol.

Calibration procedure:

- Using the LeCroy SDA 816Zi, program the DSO to capture 1MS of data at 20GS/s sampling rate.
- Select math function F1 to Difference, select input source to channel 1 and channel 2.
- In the Analysis tab, select SDA analysis function. Set PLL to off
- Setup the PeRT3 system as described in Appendix B
- In PeRT3 Protocol selection, select Generator only option.
- Program the PeRT³ to output specified data patterns and jitter values as defined in Table 2.

Transition time Validation:

- Select Math 1 of DSO to Rise2080(F1) and source as F1
- Select Math 2 of DSO to Fall2080(F1) and source as F1
- Read measure results and compare to specified range in Table 2 for Gen1, Gen2 and Gen3

Rj Calibration:

- In PeRT³ Channel Tab, select the specified Rj values for Gen1, Gen2 and Gen3
- In SDA 816Zi, go to the Analysis tab and select SDA analysis
- Setup the SDA jitter measurement and display all jitter
- Read Rj value and compare to Table 2 for Gen1, Gen2 and Gen3, adjust values to specified requirements accordingly

Sj Calibration:

- Continue from Rj Calibration
- In PeRT³ Channel Tab, select the specified Sj Amplitude for Gen1, Gen2 and Gen3. Set Sj frequency to 10Mhz
- In SDA 816Zi, read Pj value and compare to Table 2 for Gen1, Gen2 and Gen3, adjust values to specified requirements accordingly
- Validate that Pj value readings on SDA 816Zi are equivalent for 5Mhz, 33Mhz and 62Mhz.

Tj Calibration:

- Continue from Sj Calibration
- In PeRT³ Channel Tab, turn on both Rj and Sj values for Gen1, Gen2 and Gen3 accordingly
- Connect the CIC channel as defined in Section 7.2.7 of the Serial ATA revision 3.0 for Gen1, Gen2 and Gen3, adjust CIC channel length to specified requirements accordingly
- In SDA 816Zi, read Tj value (which includes Rj, Sj, CIC) and compare to Table 2 for Gen1, Gen2 and Gen3 accordingly

Amplitude Calibration:

- Set the PeRT³ Generator to output 600mV in amplitude
- Setup the LeCroy SDA 816Zi to display BER contour at 1E-12 BER level
- Setup Math measurement to measure Eye-Height at 1E-12 BER with 50% UI crossing
- Take measurement and validate it is within the specified range of Gen1, Gen2 and Gen3 requirement. Adjust amplitude at TP2 accordingly (Note, PeRT³ Generator should not output above Peak to Peak Voltage limitations for Gen1, Gen2 and Gen3 spec)

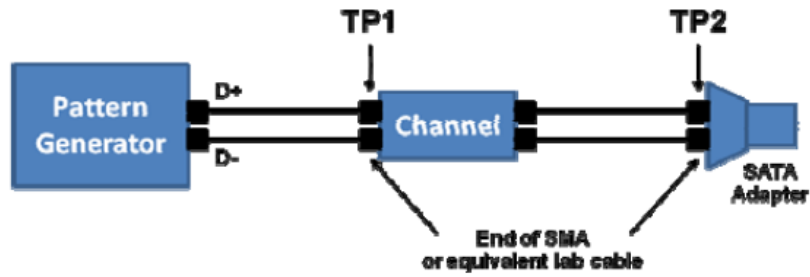


Figure 8

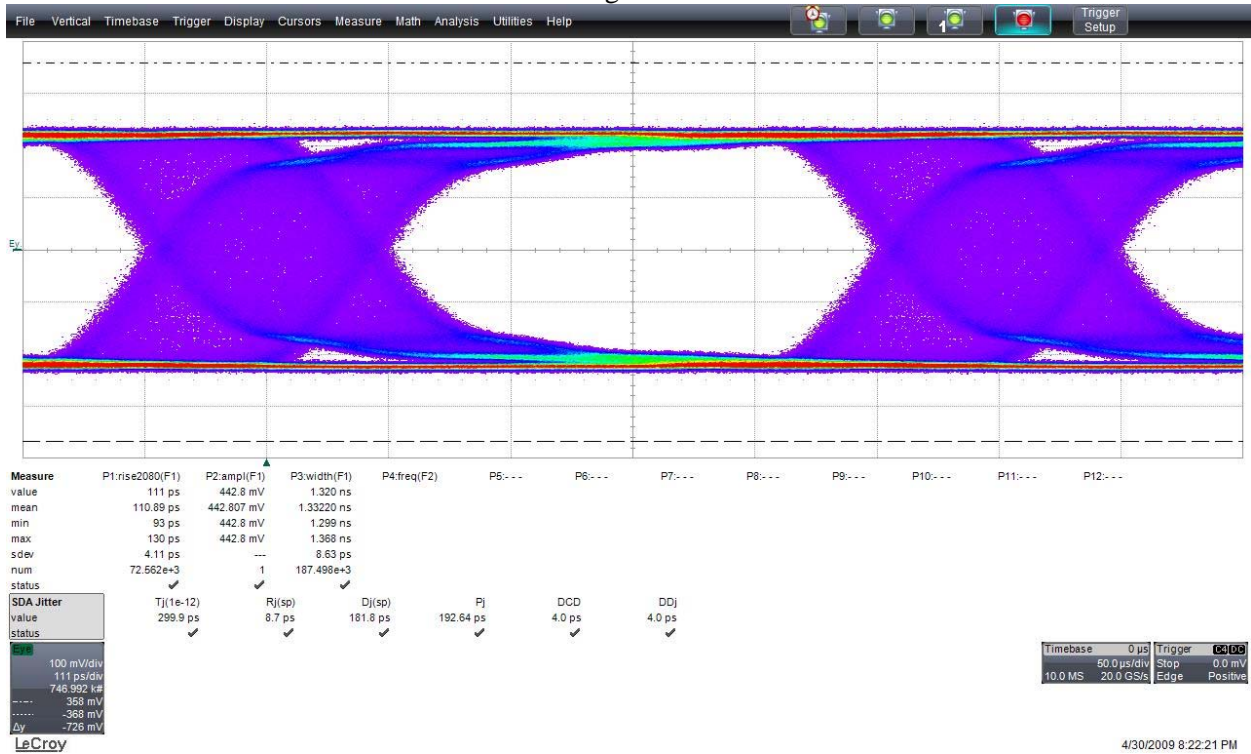


Figure 9

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Appendix D – Frame Error Rate Initialization

BIST-L Mode - Frame Error Rate Test

Purpose: Place the PUT in BIST-L to run frame error rate tests

References:

SATA Specification 3.0 – SerialATA_Revision3_0_RC2_Review1.pdf

Resource Requirements:

LeCroy PeRT³

Discussion: SATA FER (Frame Error Rate) testing can be done in either BIST-L mode or in full protocol mode. For BIST-L mode, the PUT is initialized by the PeRT³ using OOB, speed negotiation and the BIST-L FIS to put it into loopback mode. The framed COMP pattern is transmitted repeatedly by the PeRT³ and looped back by the PUT. The PeRT³'s internal SATA frame error checker counts frames and frame errors. A single frame error occurs when a frame contains one or more of disparity errors, bit errors, or invalid 10 bit codes. Multiple errors within a single frame result in one frame error. This produces an FER measurement using BIST-L mode.

Test Setup: PeRT³ connected directly to PUT

Test Procedure:

- Connect PUT to PeRT³ using SMA cables.
- Under the “Main” tab, select the desired configuration (SATA, speed, SSC).
- Set “Initialize” to Loopback and “Count” to Frame Errors.
- Click “Connect”.
- Under the “Channel Master” tab, select the desired pattern and signal characteristics.
- Click “Play” to confirm operational status.

Appendix E – PeRT³ Accuracy

Data below describes the accuracy of PeRT3 following the test procedures described in this SATA receiver tolerance MOI

RSG-01(1.5Gbps) - TBD

RSG-02(3.0Gbps) - TBD

RSG-03(6.0Gbps) - TBD

RSG-05(1.5Gbps) - TBD

RSG-06(1.5Gbps) - TBD