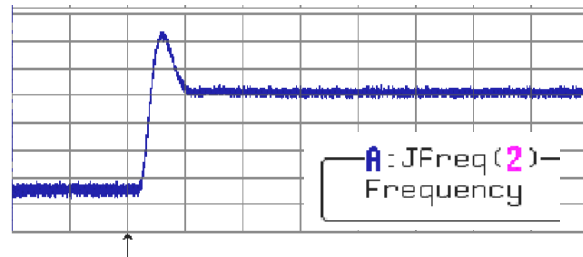
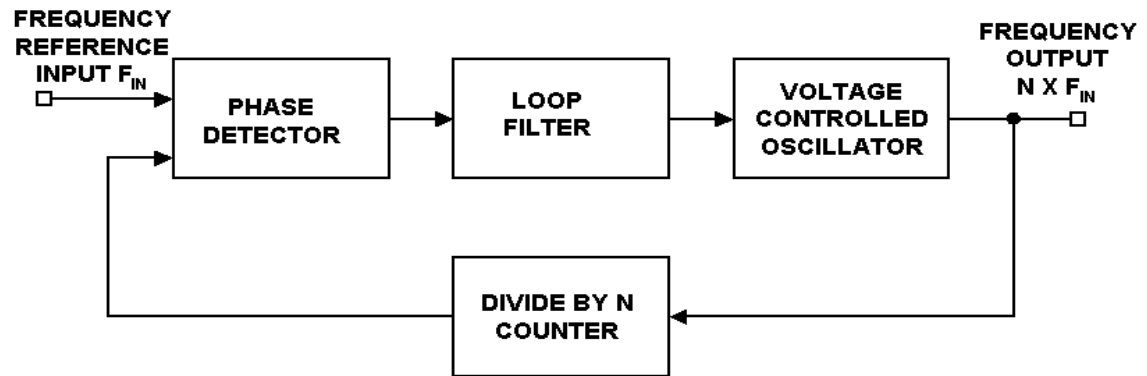


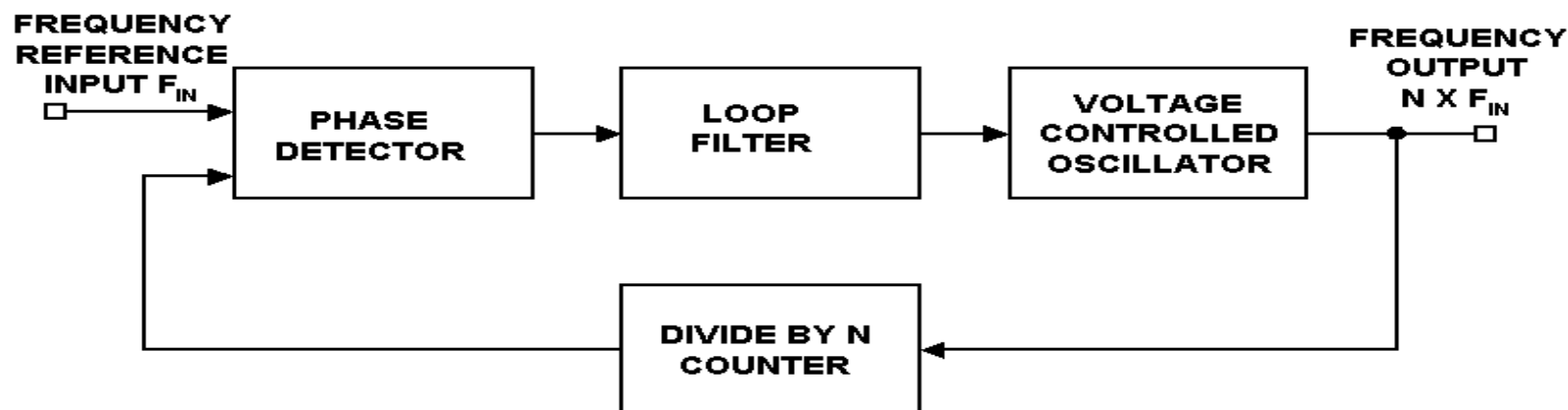
CHARACTERIZING PHASE LOCKED LOOPS



| | |
|---|--|
| FIND JITTER TRACE | use Math? No Yes |
| type Frequency 01k Data | Math Type FFTAvg Functions Jitter Histogram Per.Hist |
| of 1 2 3 4 B C D M1 M2 M3 M4 | |

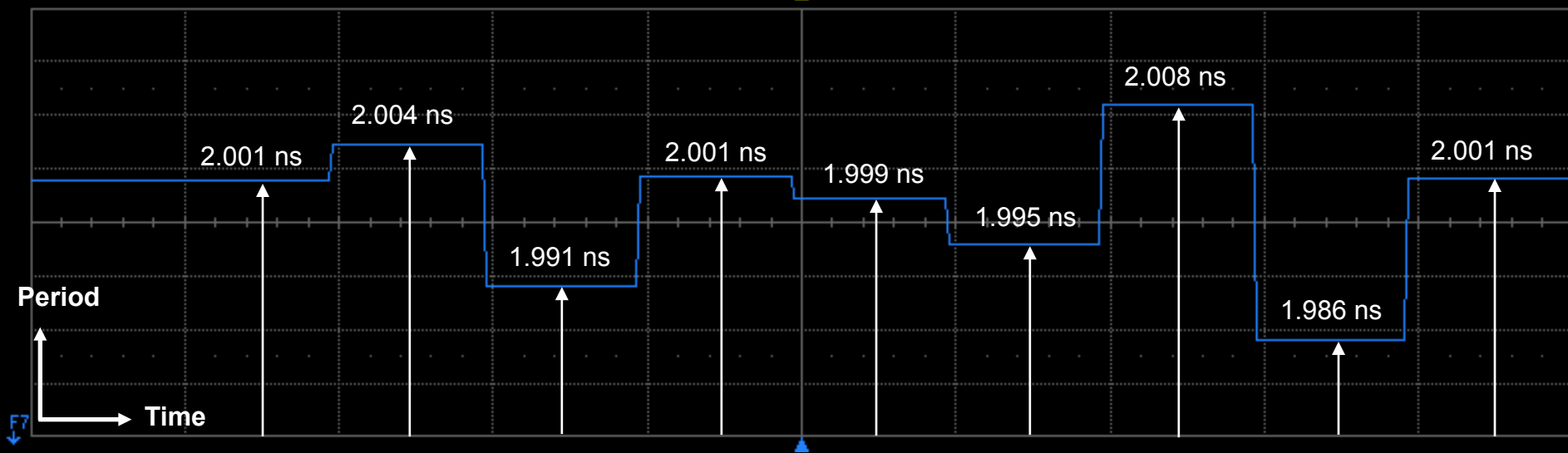
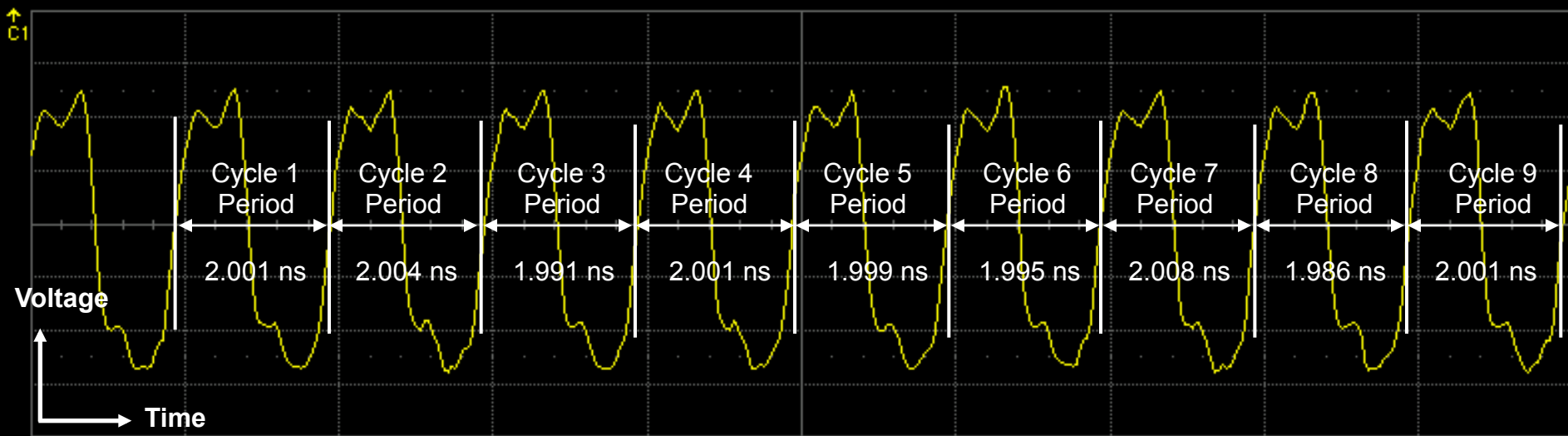


Characterizing Phase Locked Loops

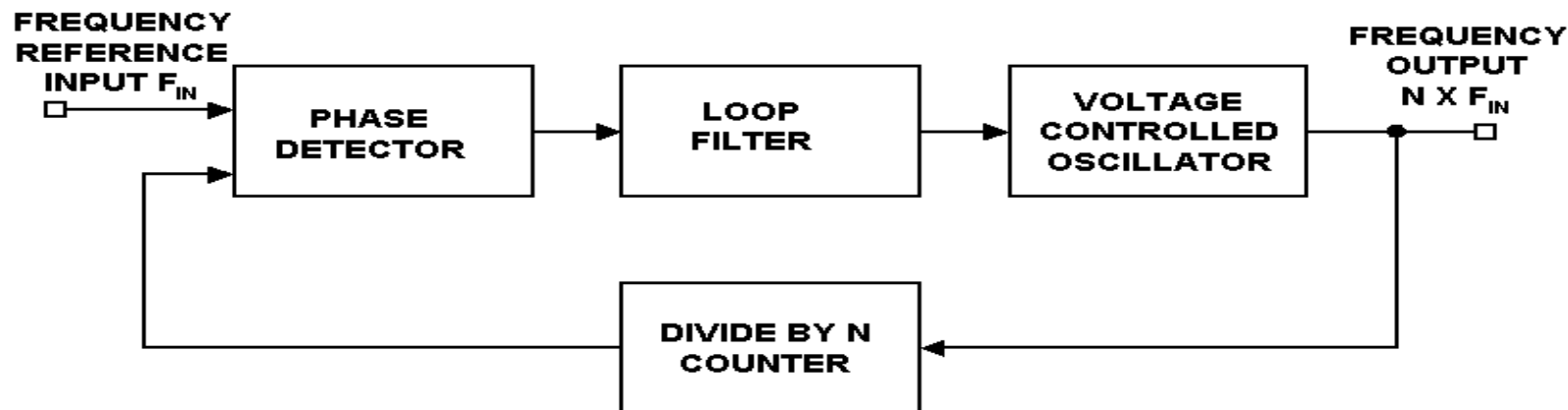


Contents:

- PLL Characterization Tools
- PLL Dynamic Response
- Method to Increase Dynamic Response Accuracy
- VCO Linearity
- PLL Loop Filter Characteristics
- Analyzing a PLL Clock Generator
- PLL Loop Bandwidth



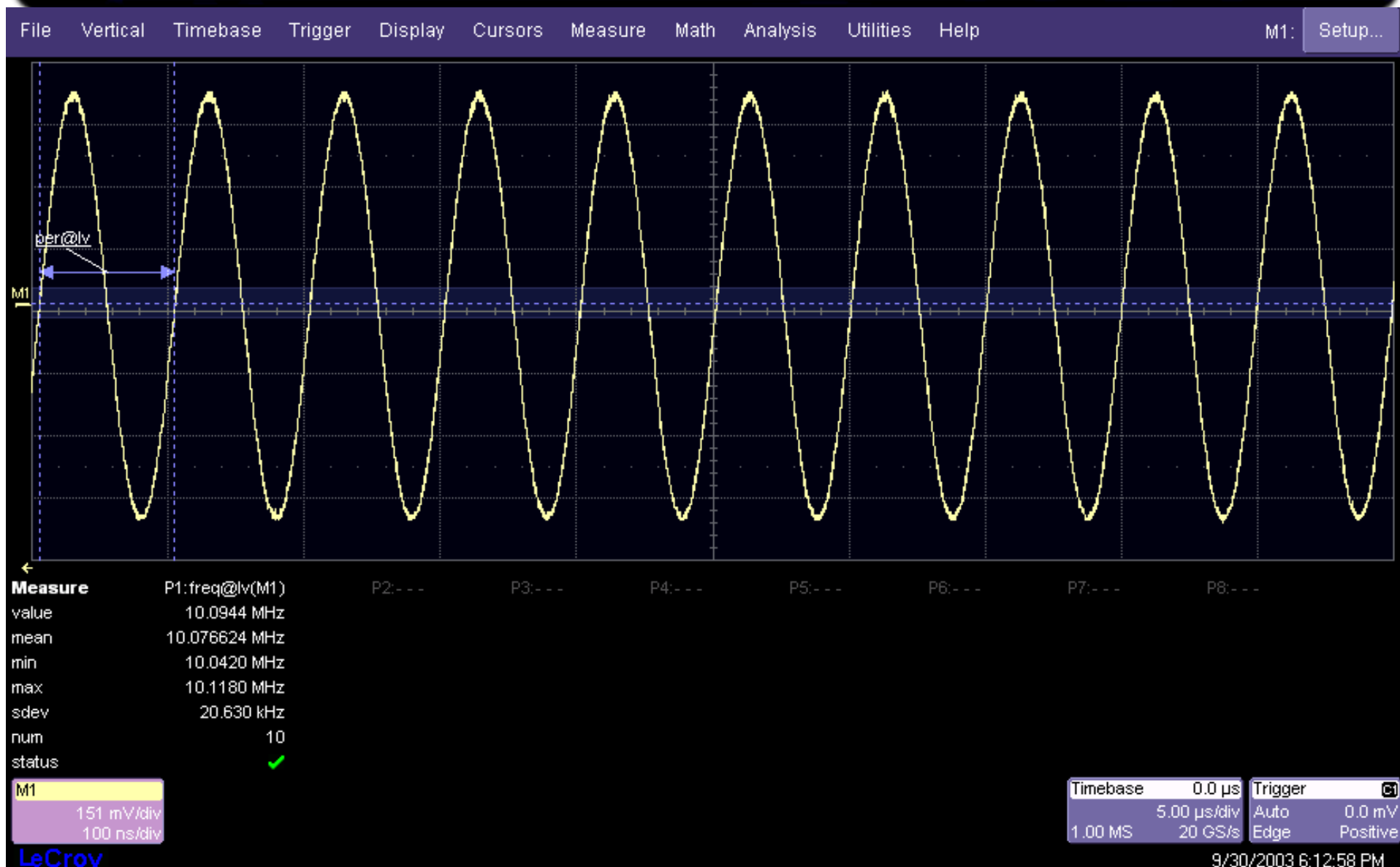
Characterizing Phase Locked Loops



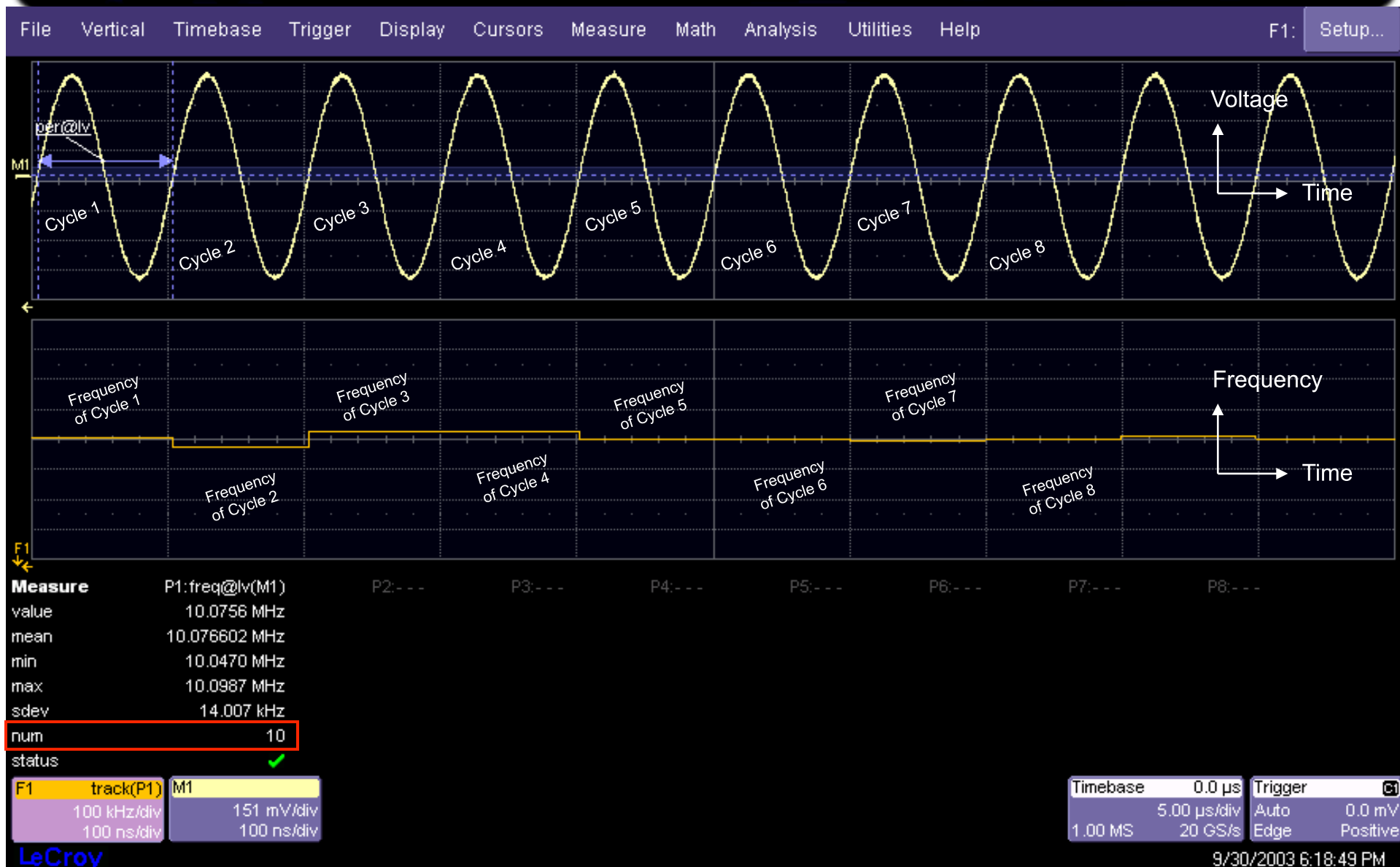
Contents:

- PLL Characterization Tools
- PLL Dynamic Response
- Method to Increase Dynamic Response Accuracy
- VCO Linearity
- PLL Loop Filter Characteristics
- Analyzing a PLL Clock Generator
- PLL Loop Bandwidth

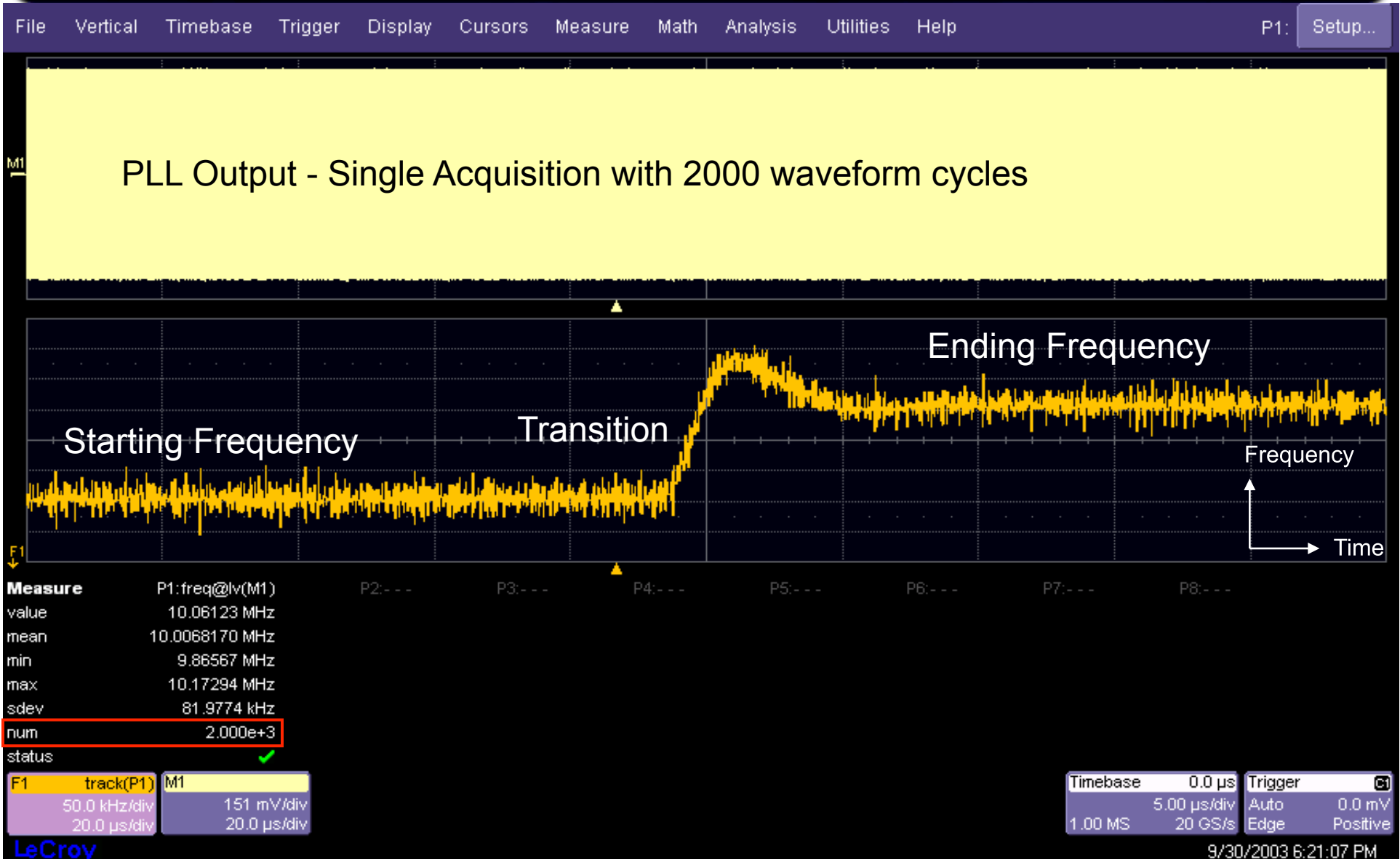
PLL Frequency Measurements



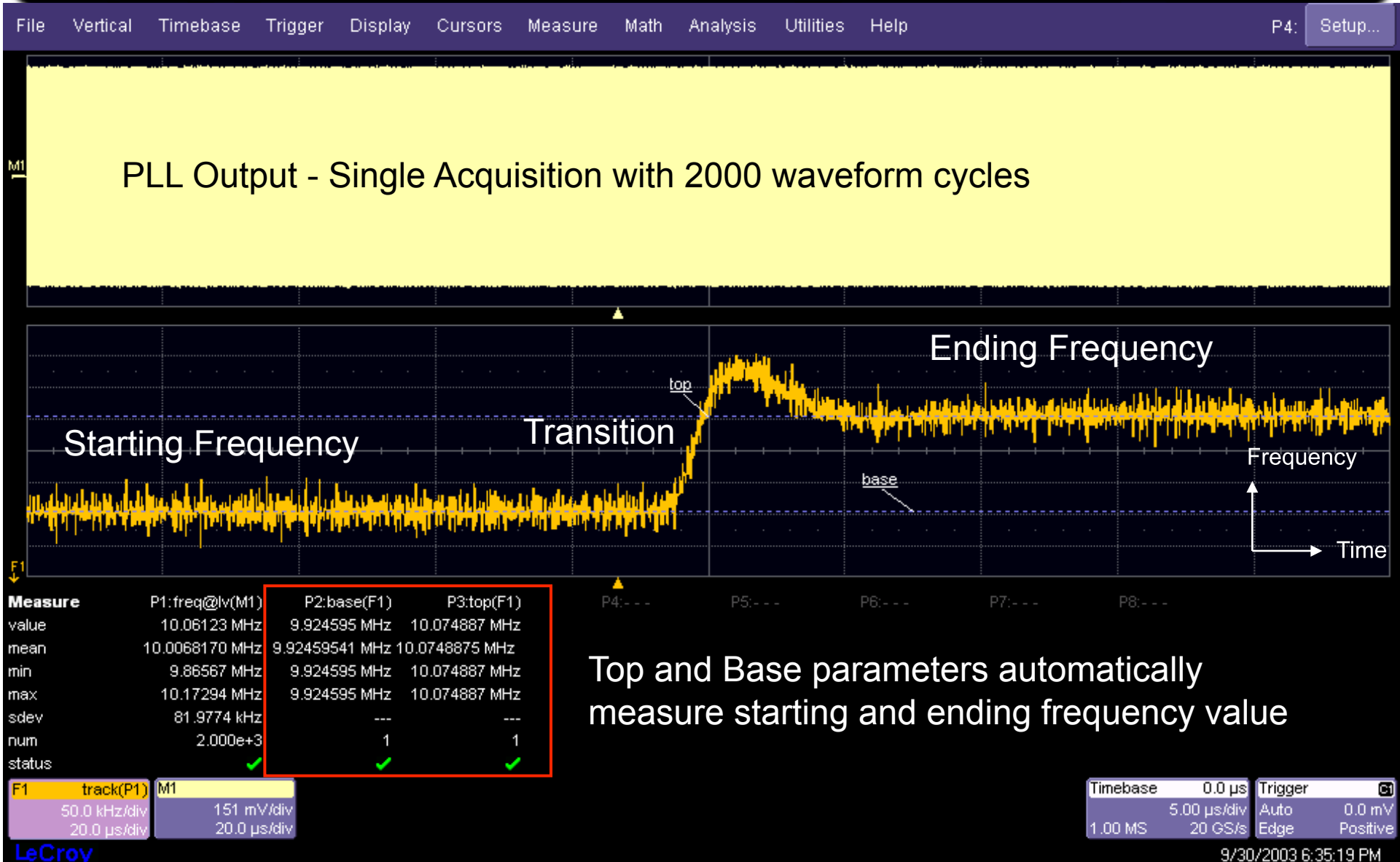
Tracking PLL Frequency



PLL Dynamic Response

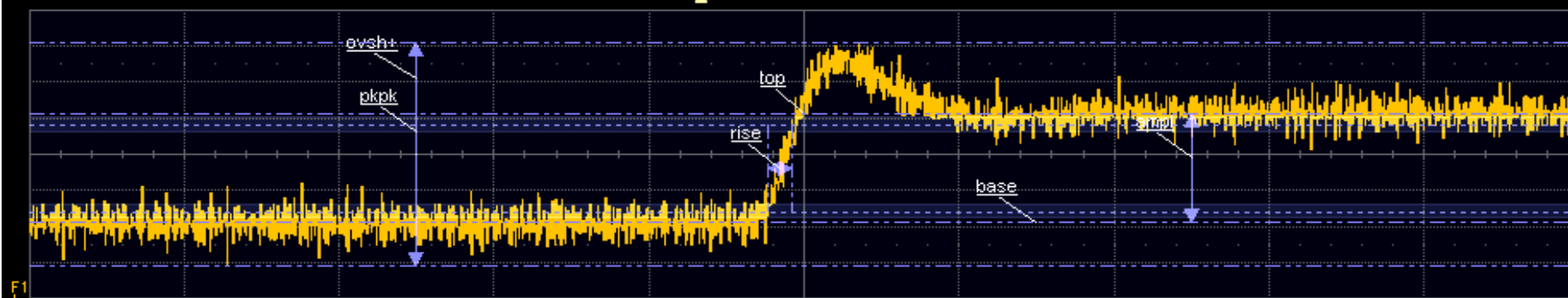


PLL Dynamic Response



PLL Dynamic Response

Risetime of Track measures transition time of PLL
 Overshoot of Track measures PLL frequency overshoot
 Amplitude of Track measures frequency transition of PLL
 PkPk of Track measures largest frequency change of PLL

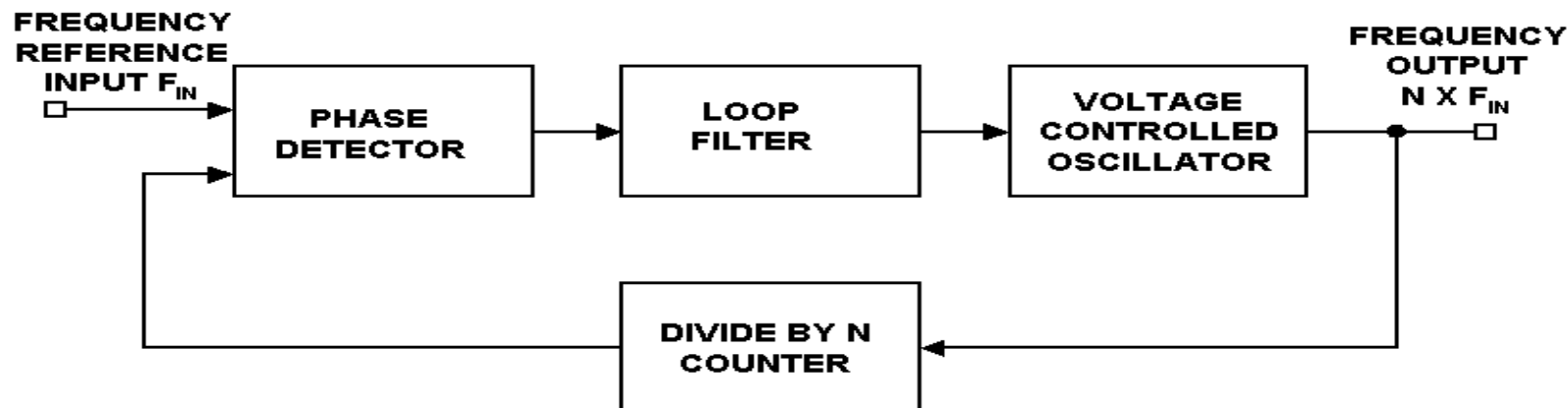


| Measure | P1:freq@lv(M1) | P2:base(F1) | P3:top(F1) | P4:rise(F1) | P5:ovsh+(F1) | P6:ampl(F1) | P7:pkpk(F1) | P8:(P7-P6) |
|---------|----------------|----------------|----------------|---------------|--------------|---------------|-------------|-------------|
| value | 10.06123 MHz | 9.924595 MHz | 10.074887 MHz | 3.101718 μs | 65.2 % | 150.292 kHz | 307.3 kHz | 157.0 kHz |
| mean | 10.0068170 MHz | 9.92459541 MHz | 10.0748875 MHz | 3.10171763 μs | 65.241 % | 150.29206 kHz | 307.273 kHz | 156.981 kHz |
| min | 9.86567 MHz | 9.924595 MHz | 10.074887 MHz | 3.101718 μs | 65.2 % | 150.292 kHz | 307.3 kHz | 157.0 kHz |
| max | 10.17294 MHz | 9.924595 MHz | 10.074887 MHz | 3.101718 μs | 65.2 % | 150.292 kHz | 307.3 kHz | 157.0 kHz |
| sdev | 81.9774 kHz | --- | --- | --- | --- | --- | --- | --- |
| num | 2.000e+3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| status | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

F1 track(P1) M1
 50.0 kHz/div 151 mV/div
 20.0 μs/div 20.0 μs/div

Timebase 0.0 μs Trigger C
 5.00 μs/div Auto 0.0 mV
 1.00 MS 20 GS/s Edge Positive

Characterizing Phase Locked Loops



Contents:

- PLL Characterization Tools
- PLL Dynamic Response
- Method to Increase Dynamic Response Accuracy
- VCO Linearity
- PLL Loop Filter Characteristics
- Analyzing a PLL Clock Generator
- PLL Loop Bandwidth

Sparsing PLL Output Waveform

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help F2: Setup...

M1 Sparse decimates its input by a factor of N, producing an output with reduced sample points

| | | | | |
|--|---|--------------------------------------|---|---|
| F1 track(P1) 50.0 kHz/div 20.0 μ s/div | F2 sparse(F1) 50.0 kHz/div 20.0 μ s/div | M1 151 mV/div 20.0 μ s/div | Timebase 0.0 μ s 5.00 μ s/div 1.00 MS 20 GS/s | Trigger Auto Edge 0.0 mV Positive |
|--|---|--------------------------------------|---|---|

Math F1 F2 F3 F4 F5 F6 F7 F8

Trace On

single dual

f(x) f(g(x))

graph web edit

Source1 Operator1

F1 sparse Sparse

Summary

sparse(F1)

Actions for trace F2

Measure Store Label Next Grid Help Markers Simple

Zoom Sparse Close

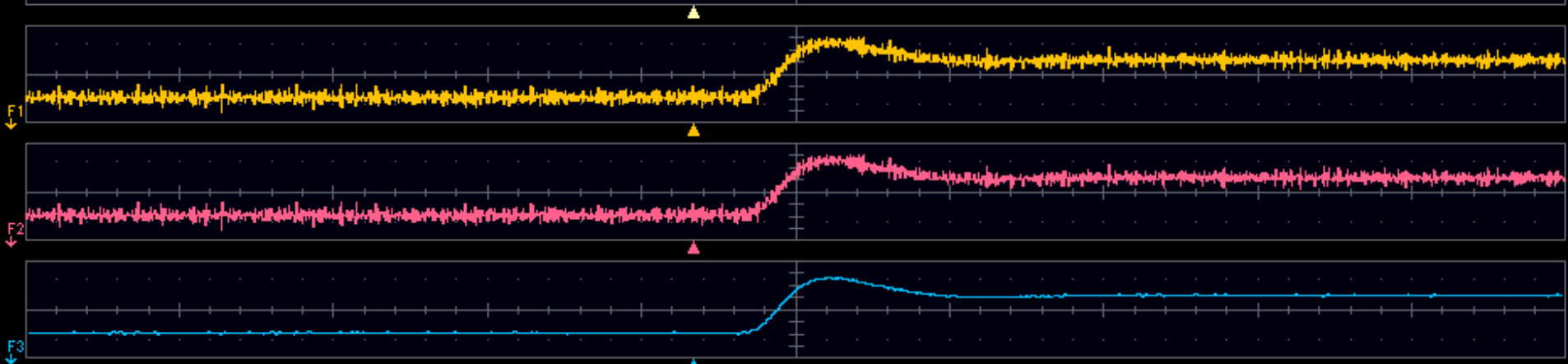
Waveform sparser, will reduce the number of points in the output waveform by skipping points in the input, and starting at a given offset.

Sparsing factor 100 Sparsing offset 0

Enhanced Resolution of PLL Output Waveform

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help F3: Setup...

M1 Eres lowpass filters its input, reducing high frequency noise and increasing resolution



| | | | | | | |
|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| F1 | track(P1) | F2 | sparse(F1) | F3 | eres(F2) | M1 |
| 50.0 kHz/div | 50.0 kHz/div | 50.0 kHz/div | 50.0 kHz/div | 50.0 kHz/div | 151 mV/div | 151 mV/div |
| 20.0 μs/div | 20.0 μs/div | 20.0 μs/div | 20.0 μs/div | 20.0 μs/div | 20.0 μs/div | 20.0 μs/div |

| | | | |
|----------|-------------|---------|----------|
| Timebase | 0.0 μs | Trigger | Auto |
| | 5.00 μs/div | | 0.0 mV |
| 1.00 MS | 20 GS/s | Edge | Positive |

Math F1 F2 F3 F4 F5 F6 F7 F8

Trace On

single dual

f(x) f(g(x))

graph web edit

Source1 Operator1

F2 Eres

Summary

eres(F2)

Actions for trace F3

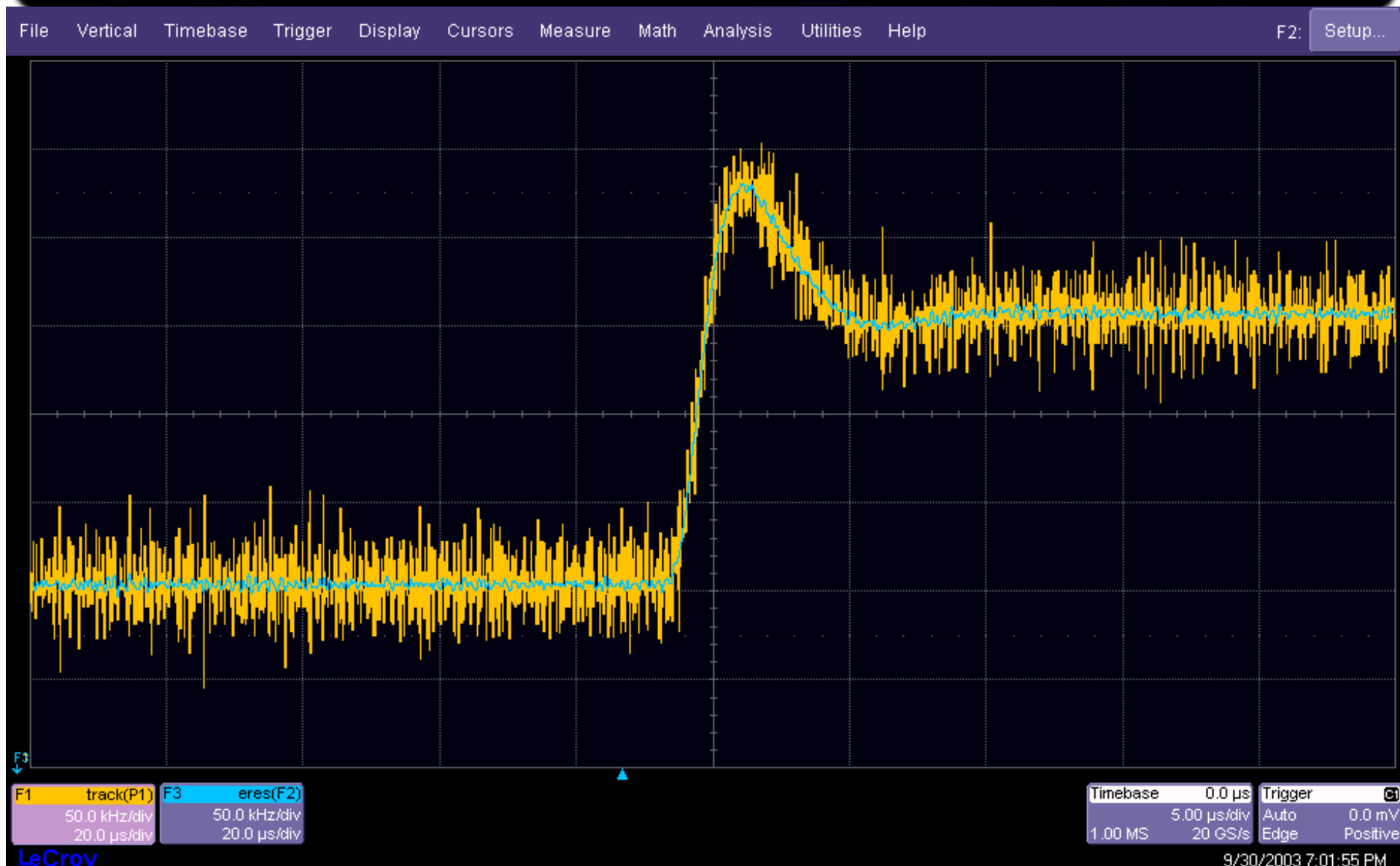
Measure Store Label Next Grid Help Markers Simple

Zoom Eres Close

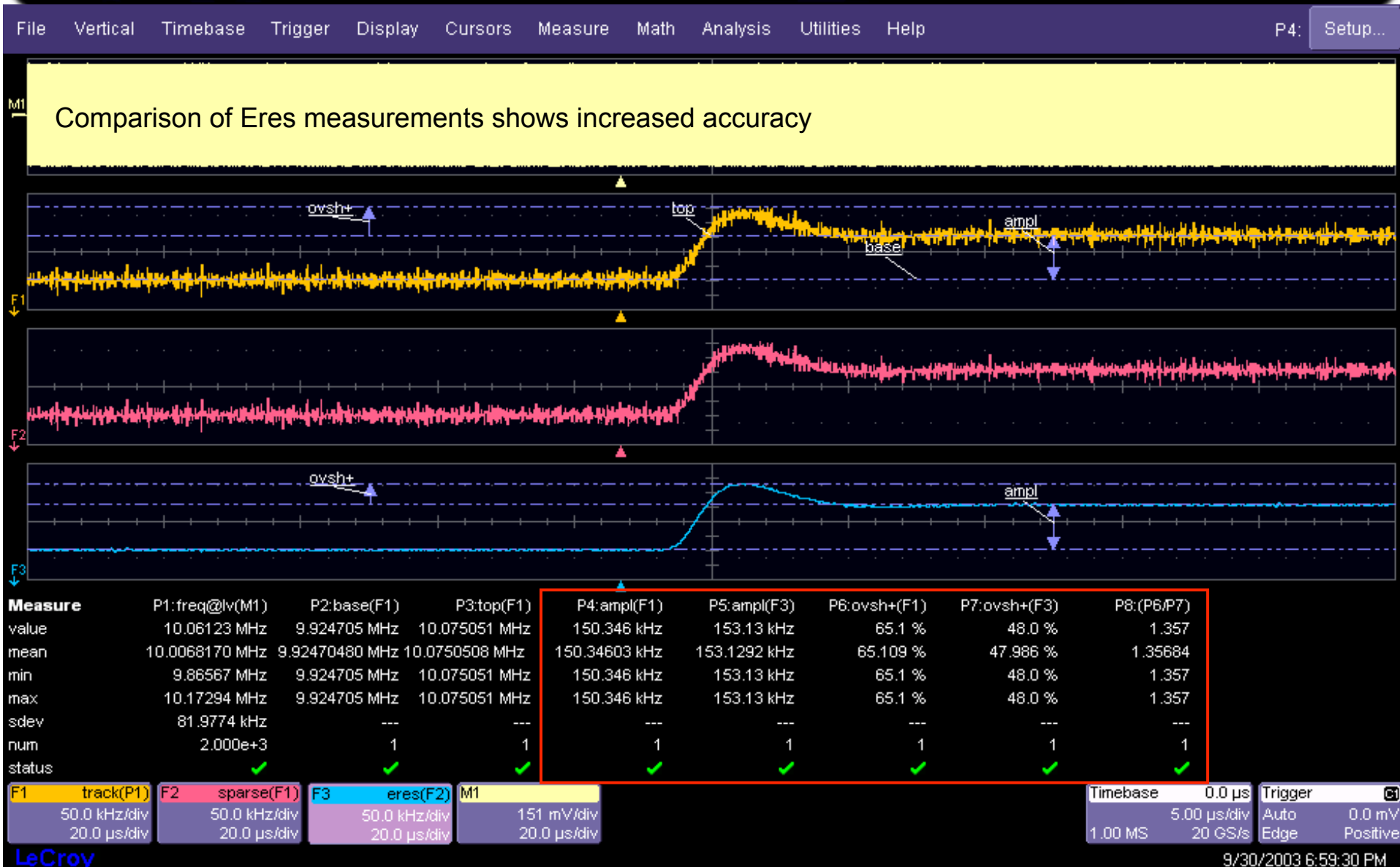
Enhanced resolution achieved through FIR filtering using well behaved filters, with precalculated noise gain.

Enhance by bits 3 taps in FIR = 106 -3dB @ 800 kHz

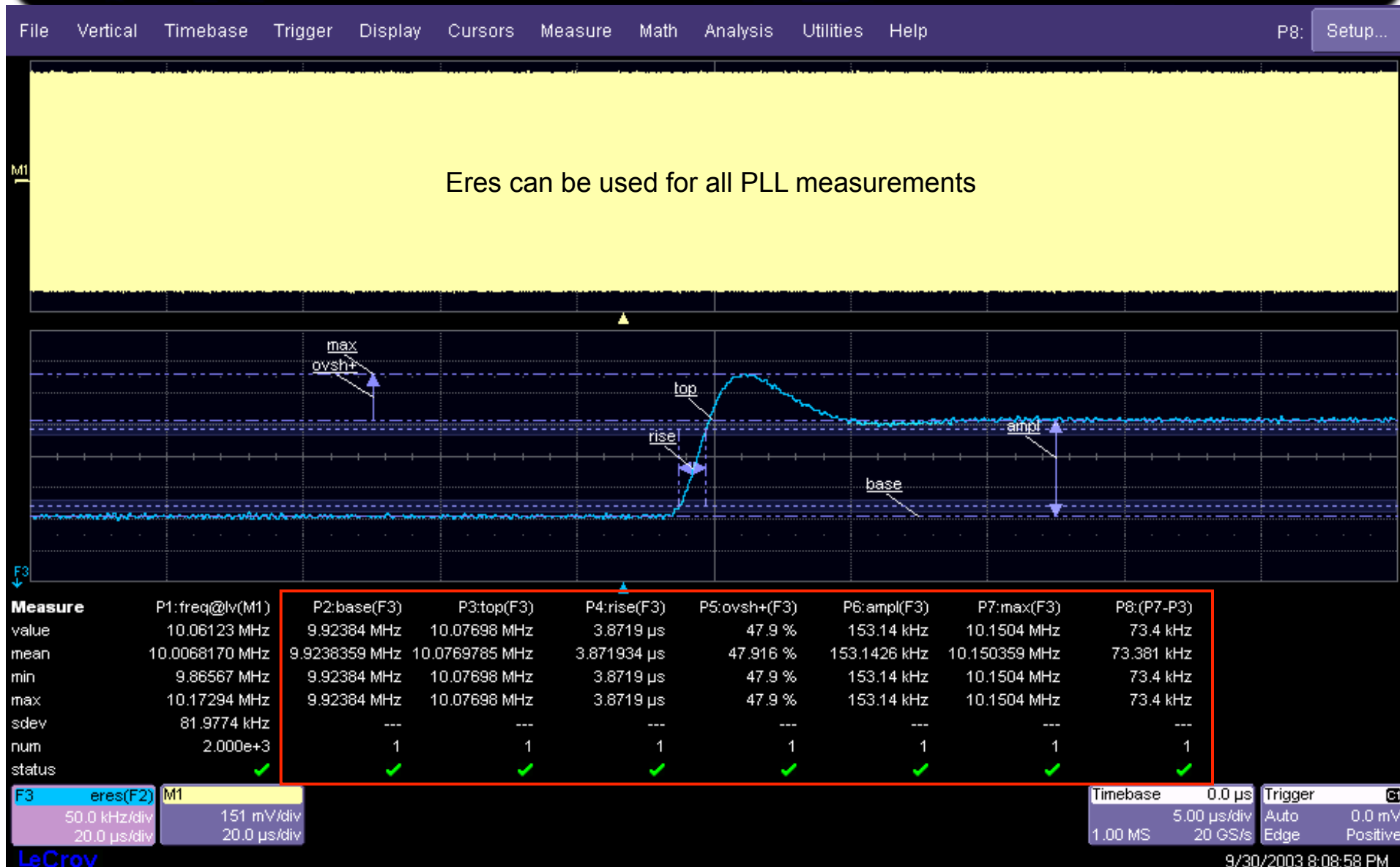
Track With Enhanced Resolution



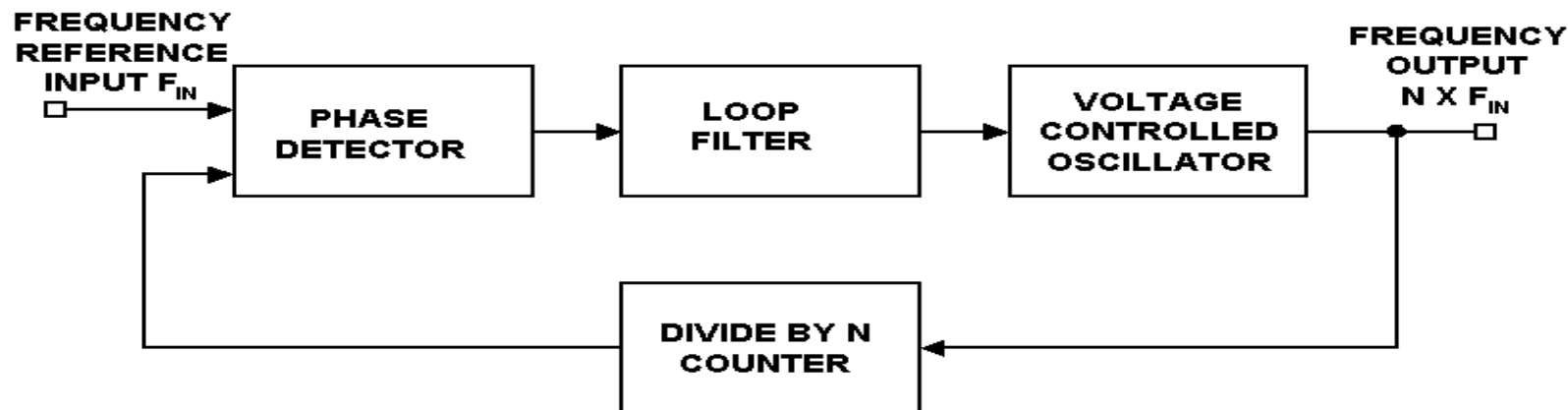
Dynamic Response Accuracy Comparison



Dynamic Response Measurements With Eres Waveform



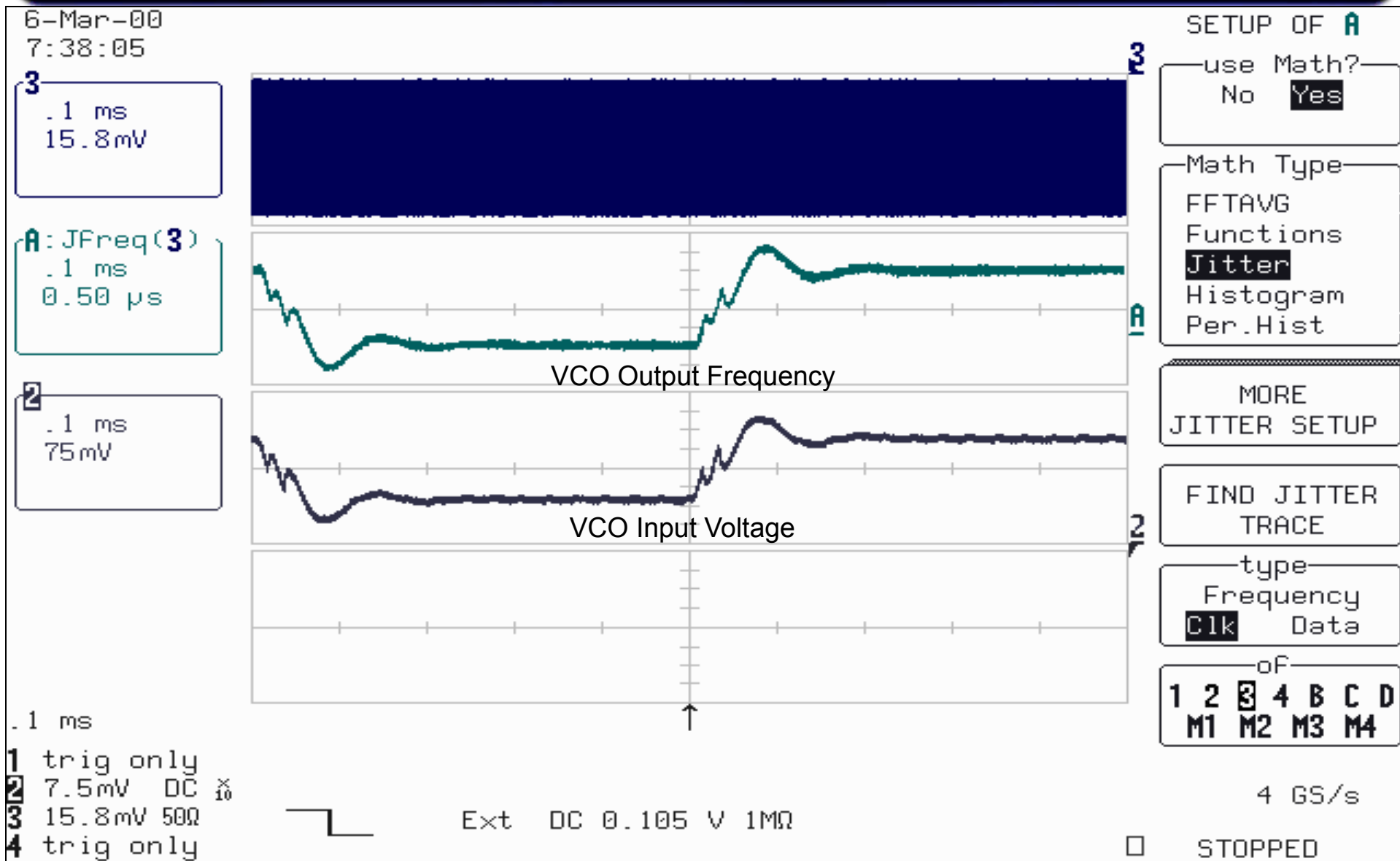
Characterizing Phase Locked Loops



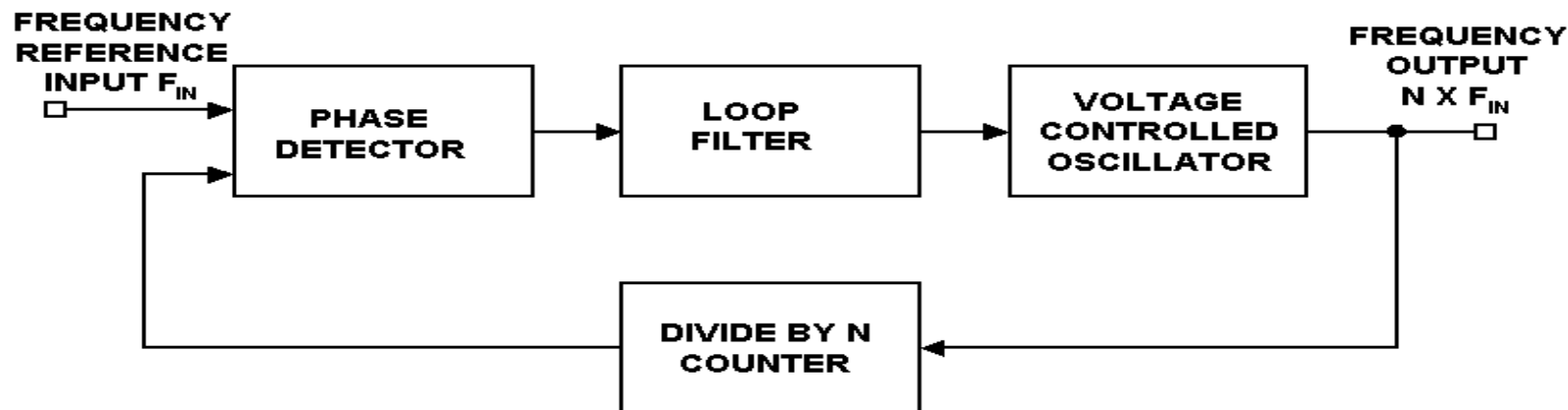
Contents:

- PLL Characterization Tools
- PLL Dynamic Response
- Method to Increase Dynamic Response Accuracy
- VCO Linearity
- PLL Loop Filter Characteristics
- Analyzing a PLL Clock Generator
- PLL Loop Bandwidth

Track to Characterize VCO Linearity



Characterizing Phase Locked Loops



Contents:

- PLL Characterization Tools
- PLL Dynamic Response
- Method to Increase Dynamic Response Accuracy
- VCO Linearity
- PLL Loop Filter Characteristics
- Analyzing a PLL Clock Generator
- PLL Loop Bandwidth

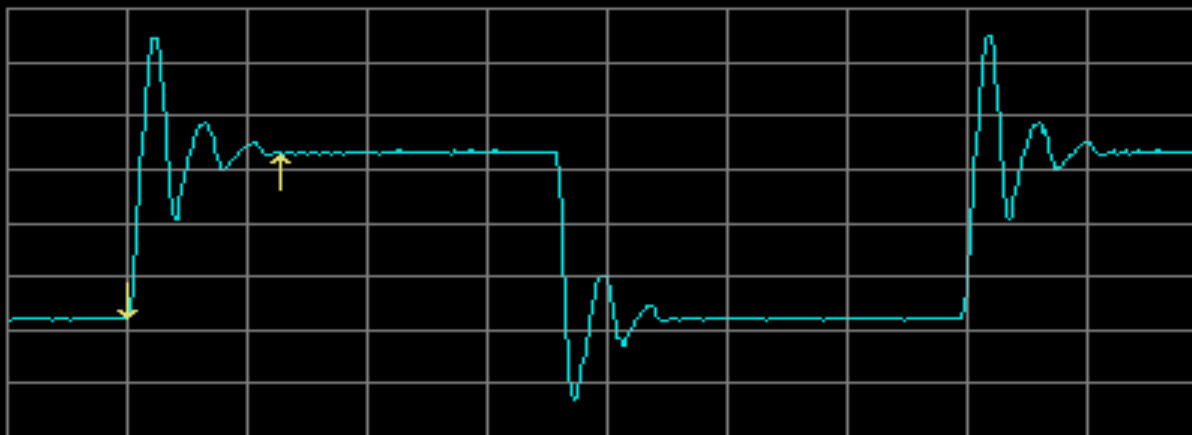
PLL Loop Filter Characteristics

28-Apr-98
10:55:48

B: Jper (3)
.2 ms
50 ns
154.61 ns

- To characterize the dynamic response of a PLL, the reference frequency input is varied between two frequencies
- The lower trace depicts the tracking behavior and settling time of the PLL output response
- By modifying the low pass filter setting, the settling time improves
- Jitter Track allow direct observation of the effects of modifying the low pass loop filter

A: Jper (2)
.2 ms
50 ns
155.80 ns



.2 ms

1 .2 V AC
2 0.84 V DC
3 1.14 V DC
4 .1 V DC

Δt 255.246 μs $1/\Delta t$ 3.9178 kHz

A: Jper (2)
Period 500000 \rightarrow 498940 pts

SETUP OF **A**

use Math?
No Yes

Math Type

FFTAvg
Functions
Jitter
Histogram
Per.Hist

MORE
JITTER SETUP

type

Cycle-Cycle
Duty Cycle
Intvl.Error
Period
Width

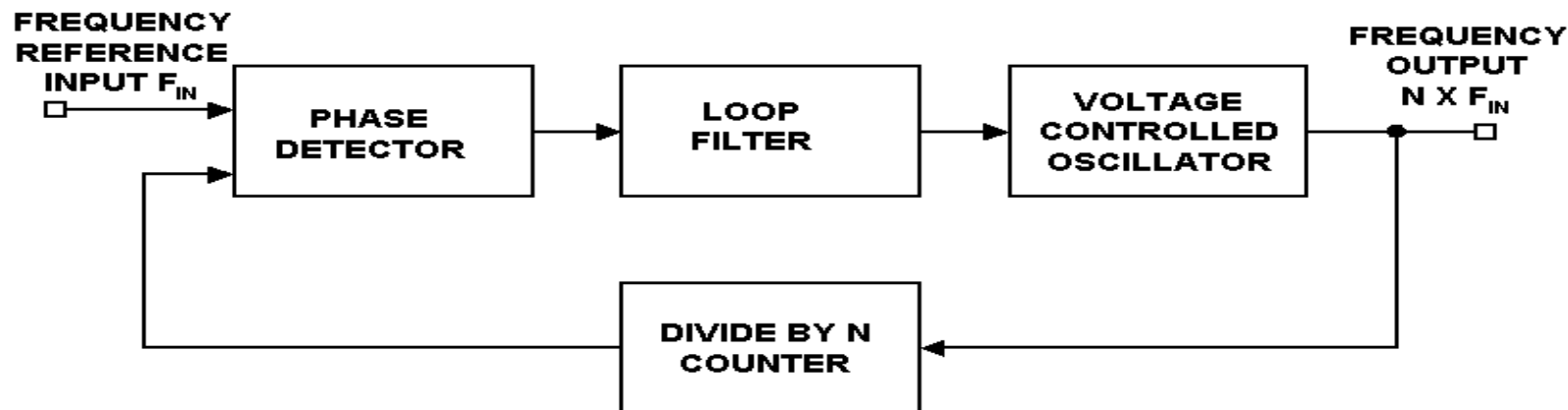
of

1 2 3 4 B C D
M1 M2 M3 M4

250 MS/s

STOPPED

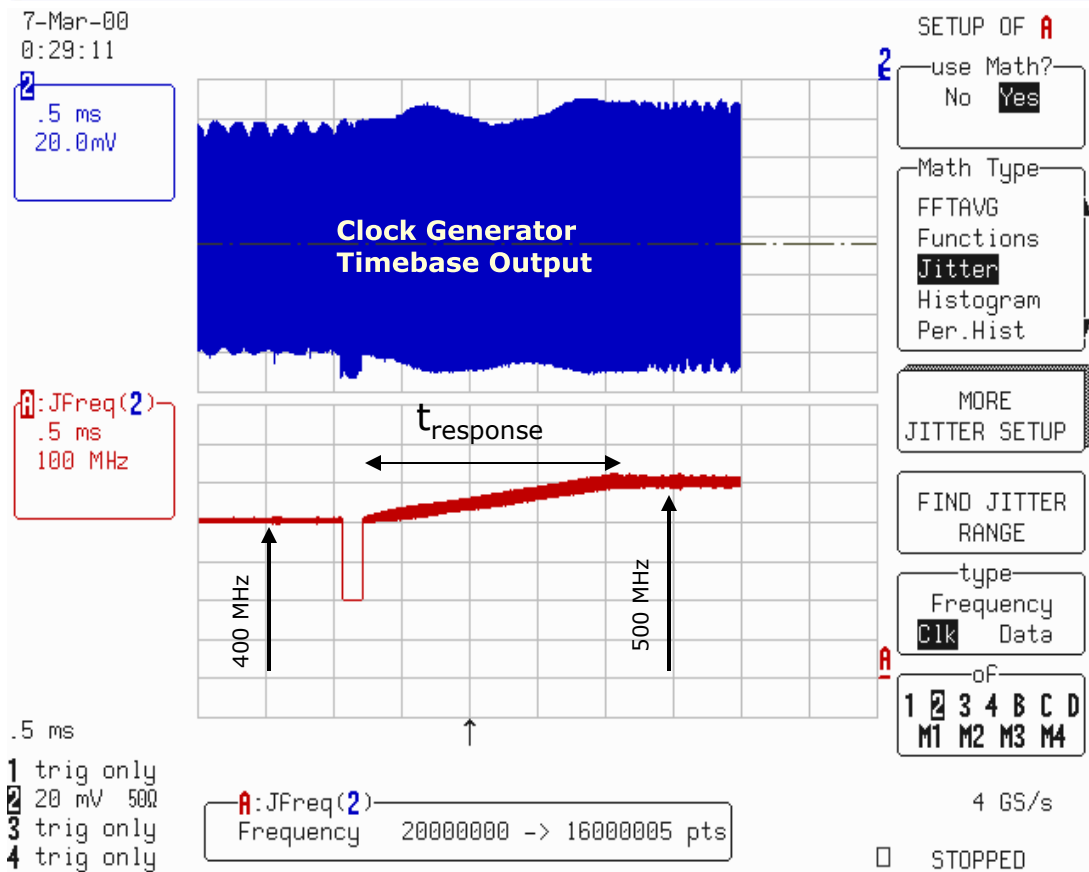
Characterizing Phase Locked Loops



Contents:

- PLL Characterization Tools
- PLL Dynamic Response
- Method to Increase Dynamic Response Accuracy
- VCO Linearity
- PLL Loop Filter Characteristics
- Analyzing a PLL Clock Generator
- PLL Loop Bandwidth

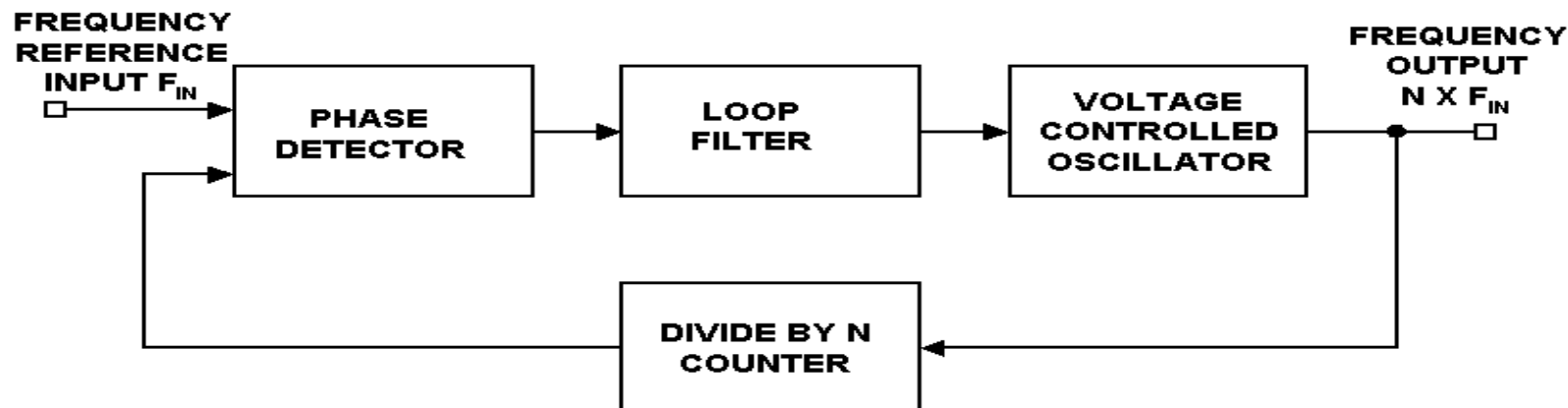
Analyzing a Phase Locked Loop Synthesized Timebase (PLL Clock Generator)



- Jitter Track can be used to study PLL response to mode changes
- The Frequency Parameter Track measures frequency modulation (FM)
- Open loop phenomena such as lock-in and capture can be measured
- Jitter Track makes it easy to study PLL tracking and dynamic response to step or impulse changes in either the reference input or of the feedback signals

Response time of a clock generator to a timebase change is characterized using the Jitter Track of frequency

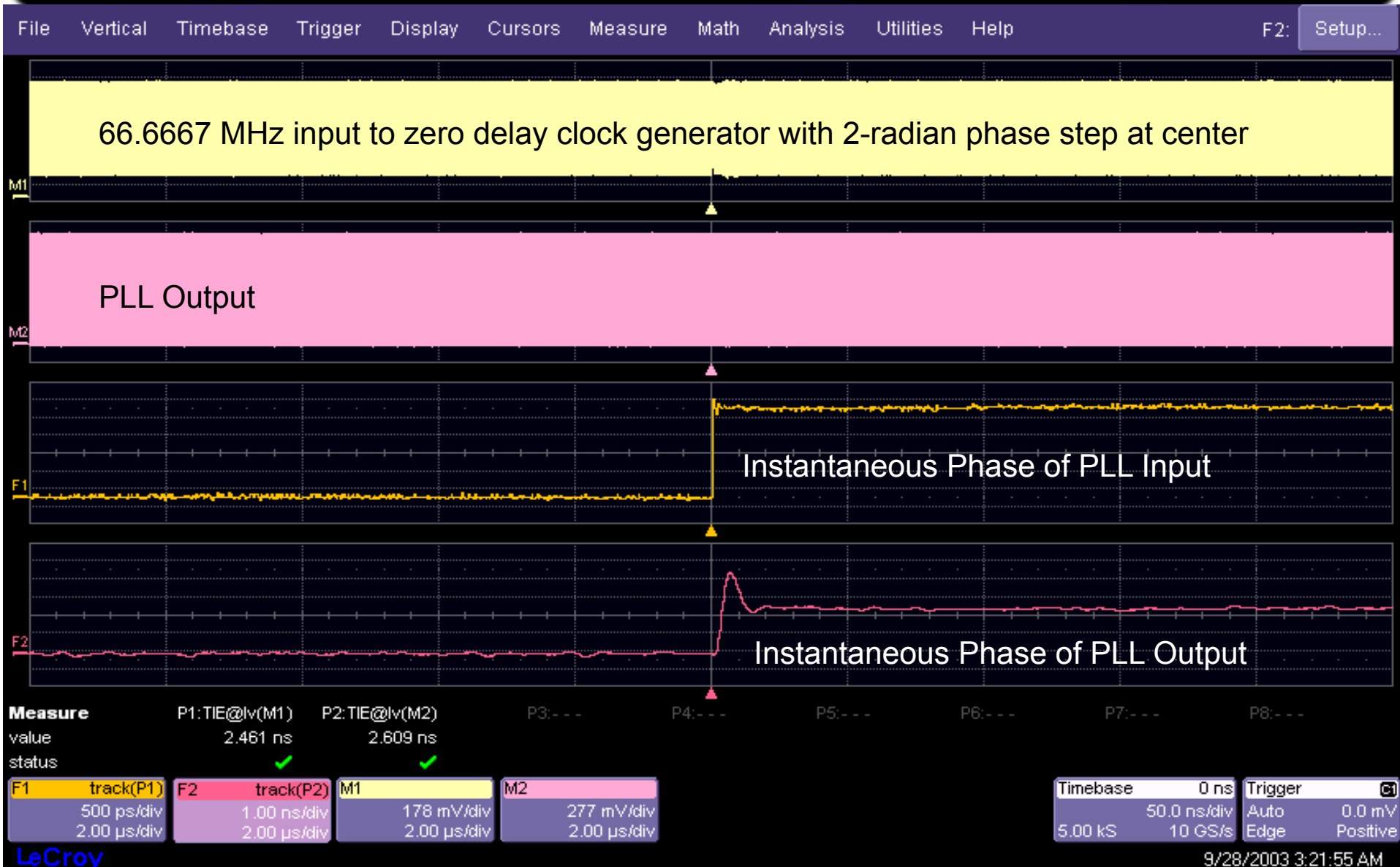
Characterizing Phase Locked Loops



Contents:

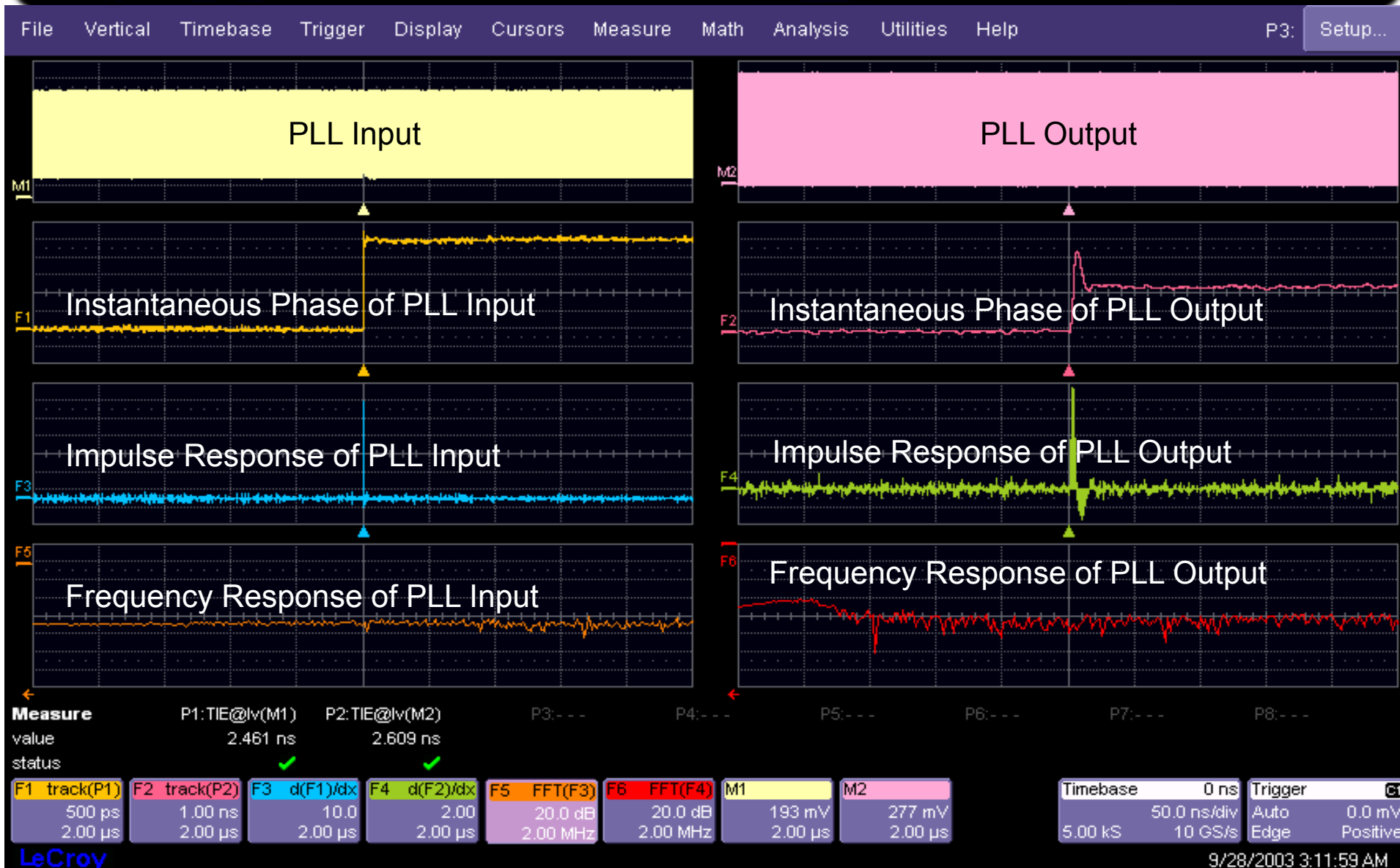
- PLL Characterization Tools
- PLL Dynamic Response
- Method to Increase Dynamic Response Accuracy
- VCO Linearity
- PLL Loop Filter Characteristics
- Analyzing a PLL Clock Generator
- PLL Loop Bandwidth

PLL Instantaneous Phase



PLL Loop Bandwidth

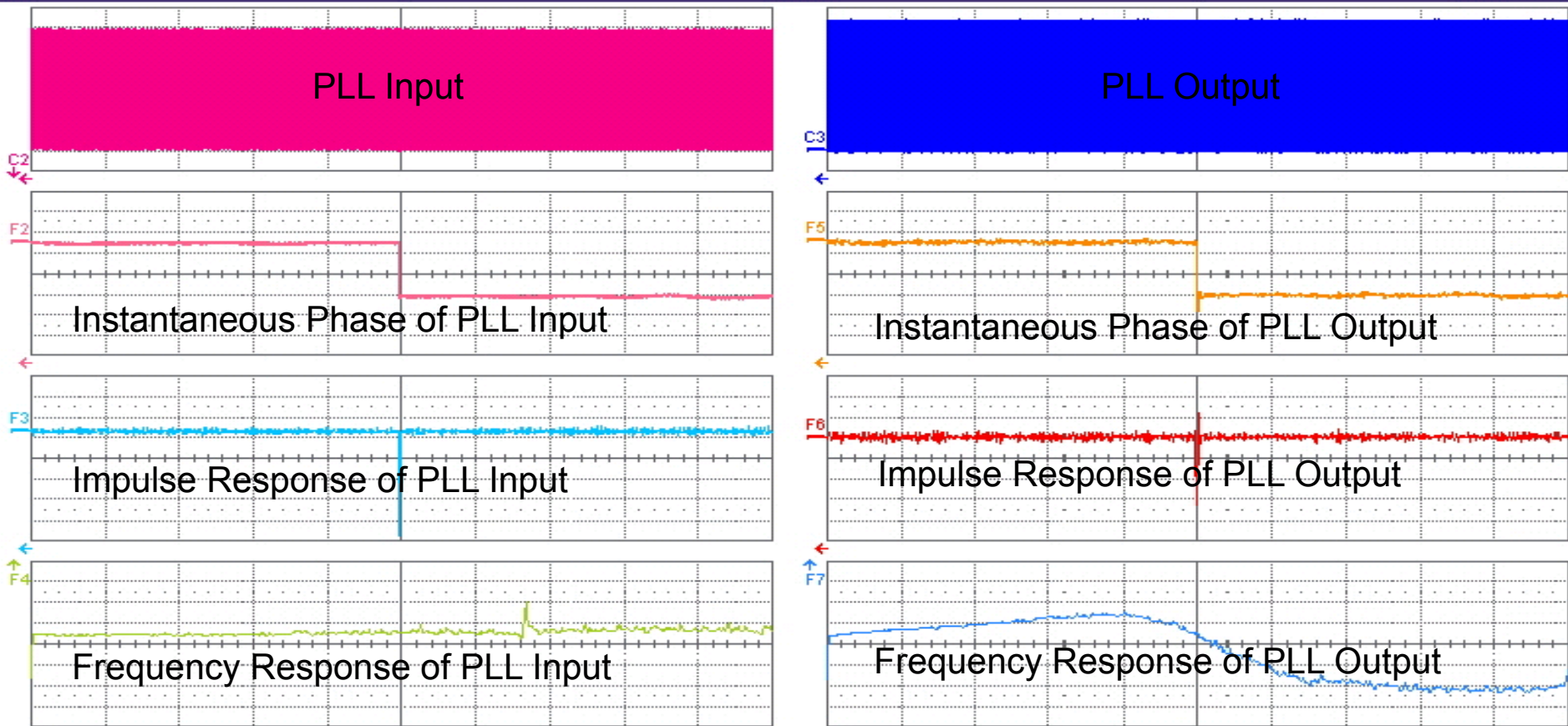
Calculating Impulse Response of PLL Input and Output Signals



PLL Loop Bandwidth with Averaging

Calculating Impulse Response of PLL Input and Output Signals

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help F5: Setup...

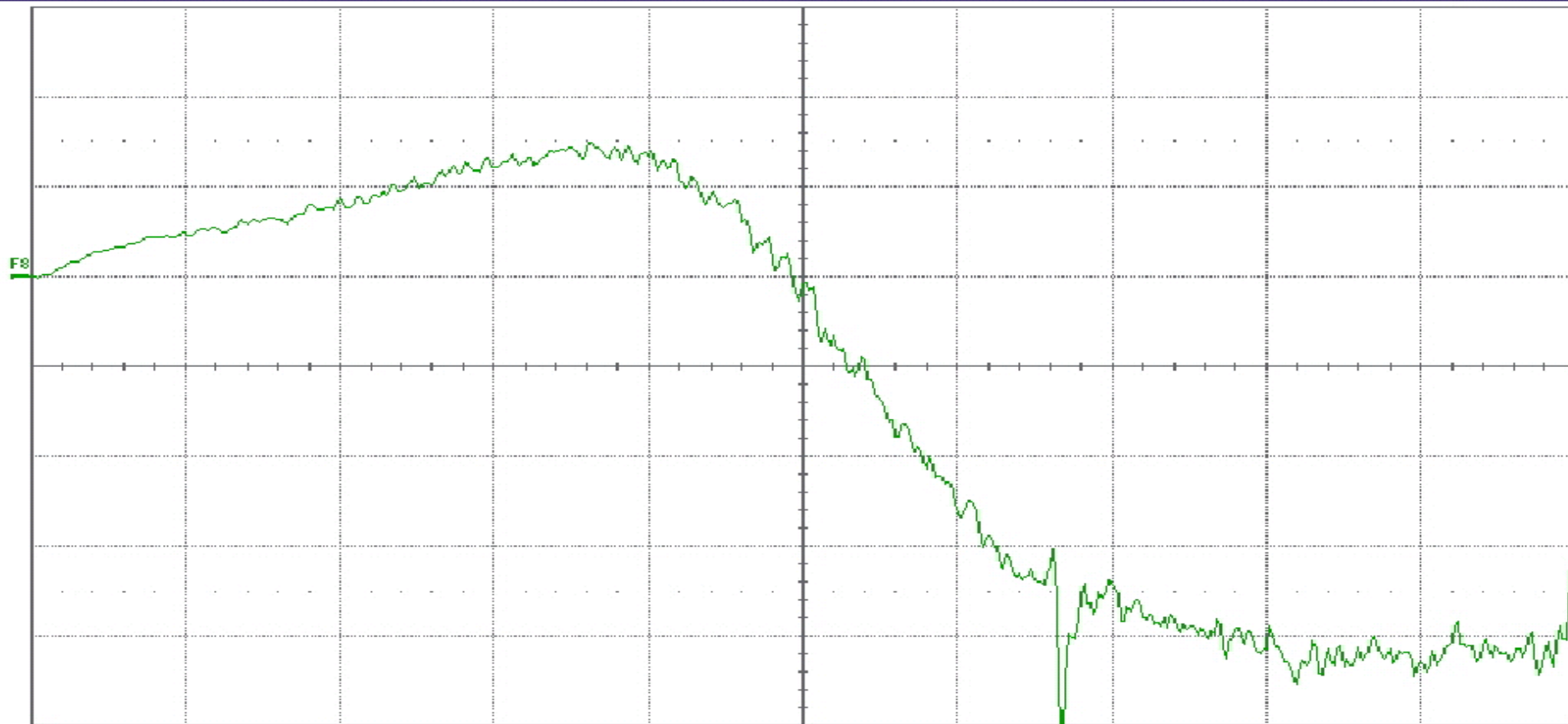


Measure value status P1: TIE@lv(C2) -2.552 ns P2: TIE@lv(C3) -2.634 ns P3: --- P4: --- P5: --- P6: --- P7: --- P8: ---

| | | | | | | | | | |
|---------|---------|--------------|----------------|---------------|--------------|----------------|---------------|------------------|------------------|
| C2 | C3 | F2 track(P1) | F3 d(spars...) | F4 <FFT(F...) | F5 track(P2) | F6 d(spars...) | F7 <FFT(F...) | Timebase | Trigger |
| 160 mV | 270 mV | 1.00 ns | 5.00e-3 | 3.00 dBm | 1.000 ns | 5.00e-3 | 3.00 dBm | -72.6 μ s | Normal |
| -694 mV | -795 mV | 10.0 μ s | 10.0 μ s | 500 kHz | 10.0 μ s | 10.0 μ s | 500 kHz | 10.0 μ s/div | DC50% Ext 145 mV |
| | | | | | | | | 2.00 MS | 20 GS/s |
| | | | | | | | | | Edge Negative |

Normalized PLL Loop Magnitude Impulse Response

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help F8: Setup...



Measure
value
status

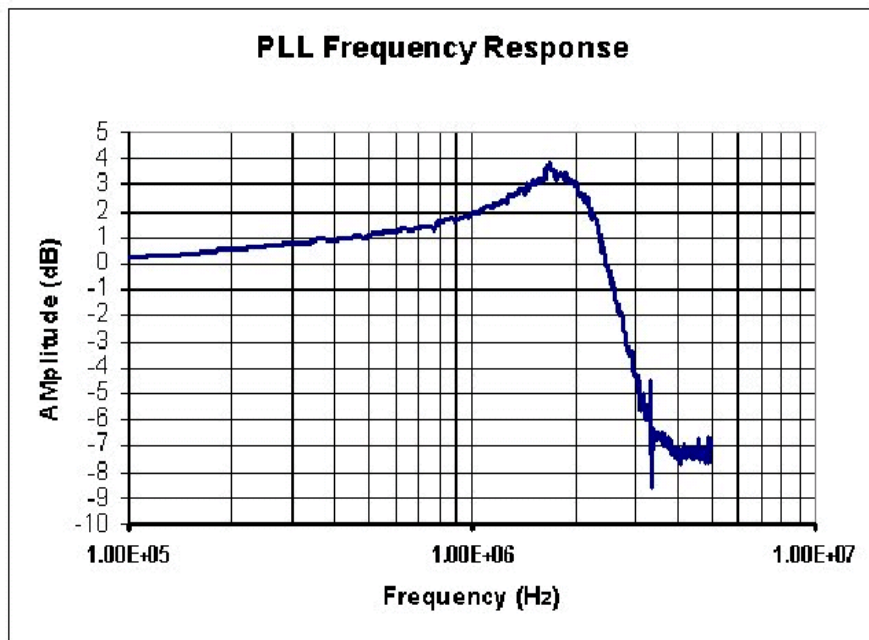
P1: TIE@lv(C2) -2.513 ns ✓
P2: TIE@lv(C3) -2.661 ns ✓

P3: --- P4: --- P5: --- P6: --- P7: --- P8: ---

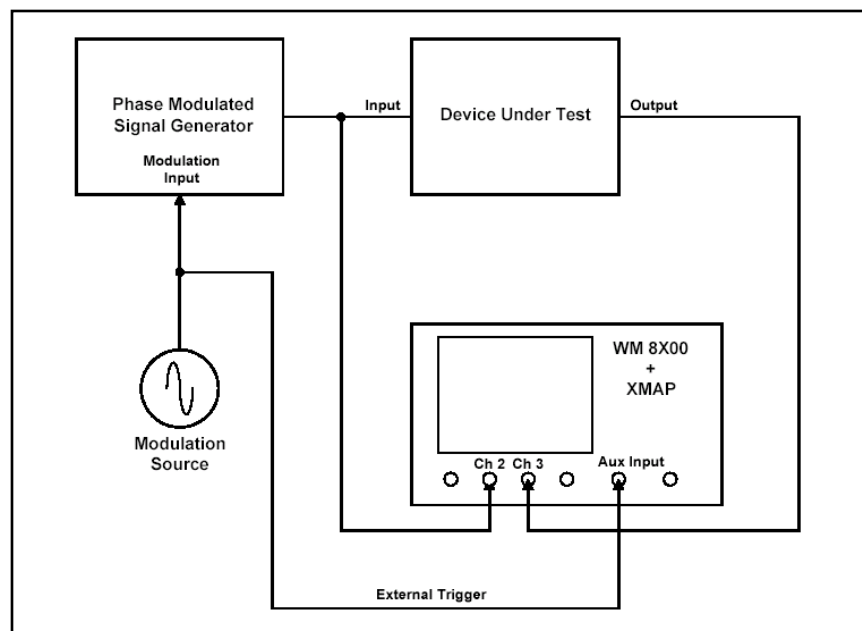
F8 (F7-F4)
2.00 dBm/div
500 kHz/div

| | | | |
|----------|------------------|---------|------------|
| Timebase | -72.6 μ s | Trigger | Normal |
| | 10.0 μ s/div | DC50% | Ext 145 mV |
| 2.00 MS | 20 GS/s | Edge | Negative |

PLL Loop Bandwidth Measurement

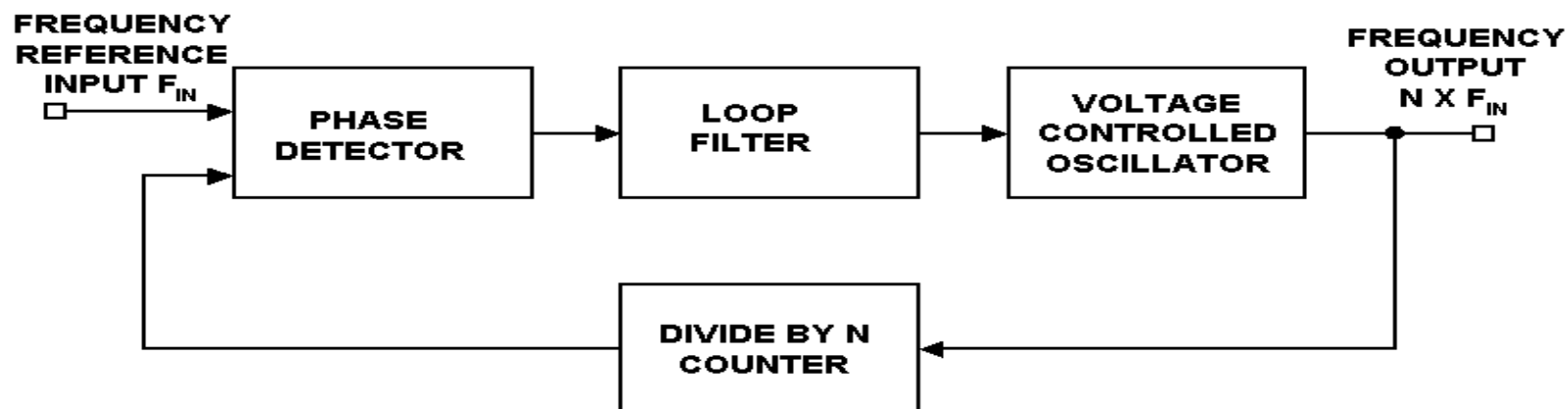


Loop Bandwidth measurement for a PLL based zero delay clock buffer



Test setup for measuring jitter transfer function

Summary



Contents:

- PLL Characterization Tools
- PLL Dynamic Response
- Method to Increase Dynamic Response Accuracy
- VCO Linearity
- PLL Loop Filter Characteristics
- Analyzing a PLL Clock Generator
- PLL Loop Bandwidth